ELEC 4707 Laboratory #3
MOSFET Diff Pair DEEP Dive

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Abstract

The purpose of this laboratory is to familiarize the class with differential pairs. In Part 1, common-mode range, gain, biasing, output resistance, and AC current flow in a differential pair are all examined. In Part 2, a differential pair is re-designed to achieve improvements in performance parameters.

I. How to Write and Submit Your Lab

A. Group Organization

Labs are to be done individually or in groups of two students. Either way, you need to enrol in a "group" for this lab on Brightspace, like you did for the previous lab. **You do need to enrol into a group again, and you don't need to keep the same partner as last time.** If you want to work alone, enrol in one of the available groups by yourself. If two students want to work together, they each need to enrol in the same group. When you want to submit your deliverable(s) for this lab, it is done by a group submission and all students in the group (either one or two students) will receive the same mark and the same feedback.

B. Deliverable Contents

The contents of your laboratory write-up should answer all questions posed in this lab write-up. **You should review the questions in advance so you are prepared to answer them and know what to look for as you conduct the lab.** Include any plots asked for in the lab, and any other plots that may be necessary for answering the questions. You should label all plots fully (titles/captions, axes, units, label different curves, etc.). If you obtain data from a plot, make the source of the data clear, and use plot markers if necessary to indicate specific plot points of interest. Of course, feel free to use Cadence tools (or any other software) to create and annotate the plots.

If you use AI to help you in this lab, include a section at the end of your report explaining how the AI was used. Please don't blindly trust the AI. Current generation AI systems are generally not trustworthy in the field of analog IC design.

C. Deliverable Format

Your lab report write-up must be done in LaTeX and must have a professional appearance. A template was given to you for the first lab, which you can use on Overleaf, and you can modify that template for this lab. You can make a free Overleaf account for this purpose. Or, if you are so inclined, of course you can run LaTeX on your own personal computer. Either way, please adhere to the format of the template in order to facilitate the marking of the labs. You can, of course, embellish as you like, but keep the order of your answers as prescribed in the template document. If you have any doubts about including things in the lab, or the format, or the required appearance of different items in your lab write-up, please throw your questions on the Discord in the appropriate channel for the lab.

Answer the numbered questions in your lab write-up. **You must start your answer for each of the numbered questions on a separate page, and clearly label which question you are answering at the top of the page. This is to make your lab easier to mark. Ensure your answers appear in the same order as the questions. In fact, to make the TAs lives easier, for marking purposes why not**

copy the questions and paste them at the top of the page and place your answers underneath? That could really help the TAs out!

D. Deliverable(s) Submission

The due date for this laboratory is one week from the date of the scheduled lab session, by 11:59pm EST. Labs should be submitted through Brightspace. Deliverables for this lab are as follows:

1) A PDF of your lab write-up with the file name `lastname.pdf` (for a one-student group) or `lastname1-lastname2.pdf` (for a two student group). Don't include dashes (-) or spaces in your name, and write all the letters in lowercase.

If the lab is submitted after midnight, 10% of the lab value is lost (e.g. 10 points are deducted from your score and the maximum mark for the submitted work is 90/100 points). Then, for each additional 24 hours the lab is late, an additional 10% of the potential lab marks are deducted (e.g. after 24 hours, another 10 points is deducted from your mark and the maximum mark for the submitted material is 80/100 points). This point deduction scheme continues regardless of weekends and holidays.

The reason we'd like the labs submitted in a timely manner is so we can mark them in a timely manner. The targeted turn-around time for marking will be one week from the submission deadline.

PART 1: PREPARING FOR THE LABORATORY.

For this lab we will again use a 45nm n-well CMOS process. The first two labs plus the tutorial should have you familiar with the process at this point in the course. If not, let us know!

II. DIFFERENTIAL PAIR OBSERVATIONS

This section is worth 70% of the lab value. After doing this part of the lab, you will be able to:

- Find the CMR of a diff-pair and choose a bias point.
- Find differential and common-mode gain.
- Sketch the directions and relative amplitudes of AC currents in the diff-pair.
- Recognize the effects of loading on a diff-pair.
- Calculate the output resistance of a diff-pair and use it to estimate diff pair gain.

A. Procedure

1) Construct the circuit shown in Figure 1. The output of this circuit is at the drain of NM1. Note that MOSFETs NM0 and NM1 are the same size (W=30μm, L=1μm), MOSFETS NM2, PM0, and PM1 are the same size, (W=30μm, L=2μm), and MOSFET NM3 has dimensions of W=20μm, L=2μm. Also note that the maximum single MOSFET gate width is 10μm in this process, so you need to enter the "total width" in the component dialog window and then Cadence will figure out the number of gates to use. Lastly, use $I_{\text{ref}} = 100\mu$A.

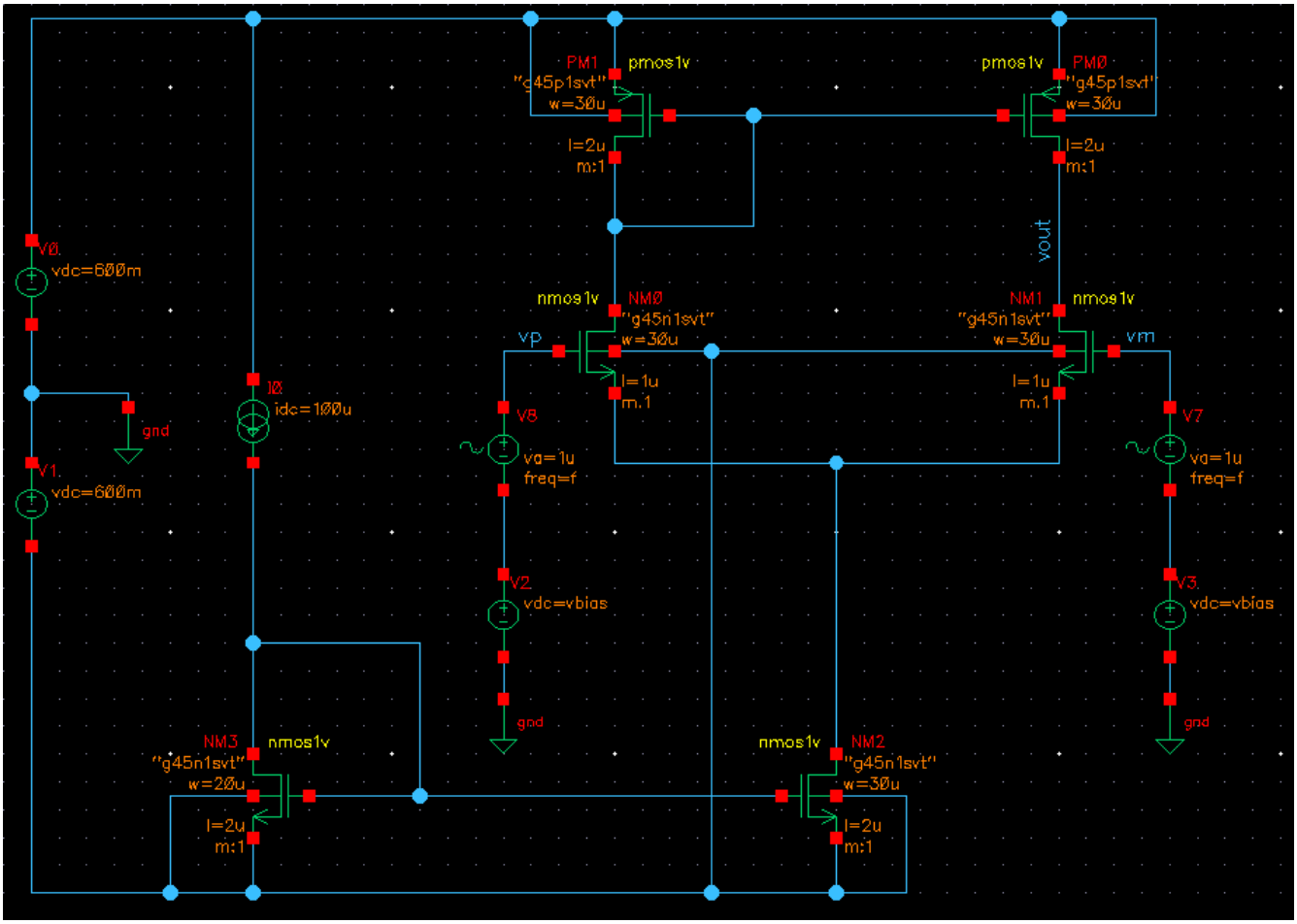

Fig. 1. The differential pair to be made in Cadence Virtuoso

Other characteristics of the circuit that should be noted are the names for the parameters inside each voltage source. set the DC voltage of the DC sources at the gates of NM0 and NM1 to VBIAS, the frequencies of each AC source to FREQ, and the amplitudes to Va

2) Sweep V_{BIAS} (use a DC sweep from the negative rail to the positive rail) to find the CMR (common-mode range). Provide plots of "region" for each MOSFET. From these plots, you can determine whether each MOSFET is "OFF" (`region=0`), in its subthreshold region (`region=3`), in its linear region (`region=1`), in its saturation region (`region=2`), or finally in breakdown (`region=4`). Once you figure out the operating region of each MOSFET from the plots you can then determine the input CMR of the amplifier (we want all the MOSFETs in saturation). Finally, provide a plot of V_{OUT} versus V_{BIAS} and annotate the plot with the upper and lower bounds of the CMR. Then also mark on your plot the theoretical results given by the equations,

$$V_{\text{BIAS,min}} \approx V_{ss} + \sqrt{\frac{2I_{ss}}{\mu_n C_{ox}\frac{W_6}{L_6}}} + \sqrt{\frac{I_{ss}}{\mu_n C_{ox}\frac{W_1}{L_1}}} + V_{T1} \tag{1}$$

and

$$V_{\text{BIAS,max}} \approx V_{DD} - \sqrt{\frac{I_{ss}}{\mu_p C_{ox}\frac{W_3}{L_3}}} + (V_{T1} - V_{T3}) \tag{2}$$

Note that you will need to find the various terms like $\mu_p C_{ox}\frac{W_3}{L_3}$. There are various ways to find those values, but perhaps the easiest is to use the simulator to save and plot the operating point value "`betaeff`". In Cadence, `betaeff = ueff * coxe * weff / leff` where `weff` and `leff` are the effective width and length of the MOSFET. We discussed in class how the drawn

length (what you would draw using the layout editor in Cadence for the MOSFET gate) differs from the actually manufactured gate's width and length. Cadence makes an estimate of the probable effective width and length accounting for manufacturing effects. Anyway, the bottom line is you can use `betaeff` for the $\mu_p C_{ox} \frac{W_3}{L_3}$ types of terms (there is a different `betaeff` for each MOSFET). The value of `betaeff` is bias dependent but it doesn't vary that much so you can use the value around the midpoint of your CMR that you can ballpark visually.

Deliverables for this part: [5 points] Region plots; [5 points] V_{OUT} versus V_{BIAS} plot with CMR shown, and brief explanation of how the CMR was determined from the plots; [5 points] additional annotation of theoretical CMR on V_{OUT} versus V_{BIAS} plot, and include the calculations of the CMR end-points. Comment on why there is a difference between the calculated values and the simulated values (there will be a difference!) [5 points] Also, what is the static power dissipation of this circuit? What could you change to increase or decrease it? What are some of the possible trade-offs, if any, that could occur from the changes you describe?

3) Set V_{BIAS} to the mid-point of the CMR found in step 2 (using the region plots, not the theoretical equations). Add a 10MΩ load resistor (`res` component from `analogLib`) between the output node and ground. Set both sinusoidal sources to have an amplitude of 1μV and frequency 1 Hz, and ensure they are in-phase (common mode). Run a transient analysis over a time interval of 1 second. **Deliverables for this item: [5 points] Provide a plot of the simulation result (plot vm, vp, and vout on separate strips); [5 points] Calculate the common-mode gain and provide the calculations.**

   Next change vm so that it is 180 degrees out of phase with vp. Re-run the transient. **Deliverables for this item: [5 points] Provide a plot of the simulation result (plot vm, vp, and vout on separate strips); [5 points] Calculate the differential-mode gain and provide the calculations. [5 points] Based on the common-mode gain, and the differential mode gain, what is the common-mode rejection ratio (CMRR) of the differential pair? Give the answer in dB. [5 points] Next, complete a Monte Carlo simulation and provide a histogram of how the CMRR varies depending on how the devices change. An example of what your histogram should like like is provided in figure 2. In your histogram make sure to have 200 points. You are free to do this simulation using whatever setup you like, make sure to explain how you set it up. Also, INCLUDE YOUR NAME AND STUDENT NUMBER ON YOUR HISTOGRAM PLOT BY PUTTING IN TEXT IN CADENCE. An example of one method you can use is to set up two simulations, an AC analysis and a transient analysis. You can use the transient analysis to get your common-mode gain and the AC analysis to get your differential gain. You will need to set up the DC input sources for the differential pair to include an AC magnitude and AC phase and set the sinusoidal voltage sources to generate the common-mode signals, as you did before. You can use calculator expressions to extract the CMRR from these two simulations. Comment on your results and your method. Also, as a hint, some useful functions you may wish to use to help get the required data for the CMRR are the deriv, ymax, and value functions in the calculator. If you need help setting them up, select them and then press the 'help' button at the bottom of the calculator for an in-depth explanation of how the function works and its required inputs**

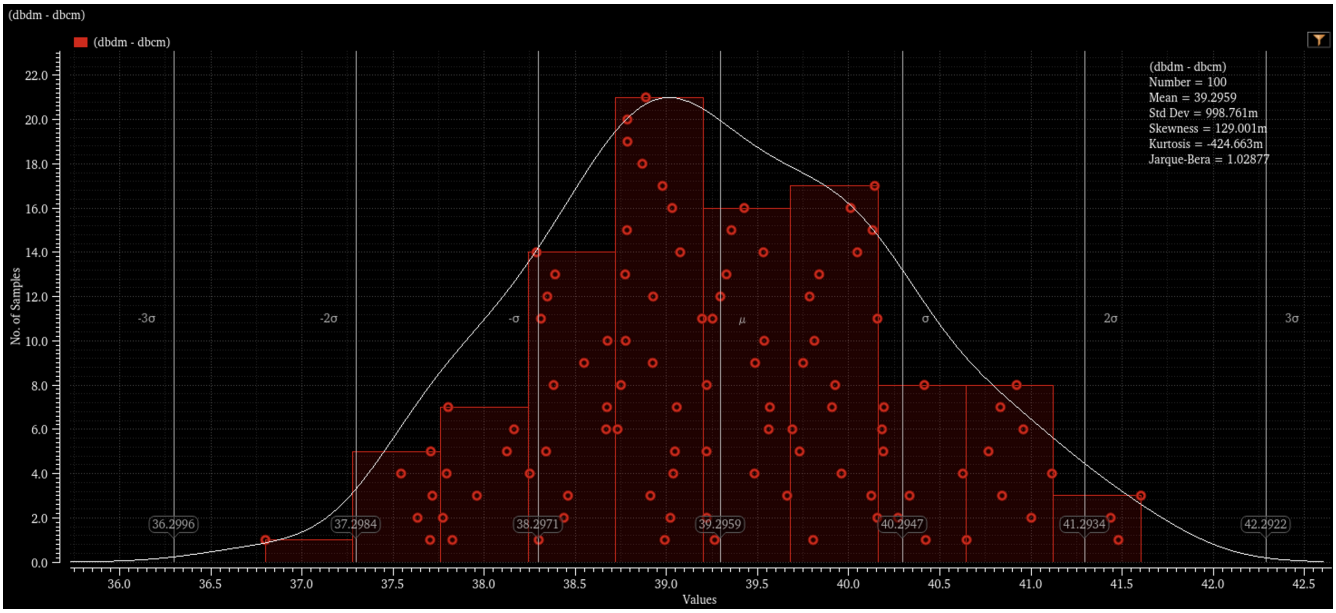

Fig. 2. A histogram made through a Monte-Carlo simulation testing the CMRR

4) Set the load resistance to 1kΩ. Set the amplitude of vm to zero. Re-run the transient. **Deliverables for this item: [10 points] Provide plots of the currents flowing into the drain of the nmos devices, and the source of the pmos devices. Annotate the schematic by adding RED arrows representing the direction of small-signal current flow, assuming that the small-signal current in NM0 is the reference (e.g. the phase of the current in NM0 is the reference phase). For currents that are approximately zero compared to other currents, indicate that these currents are "very small".**
5) Replace the resistor load with a 1pF capacitor (`cap` component from `analogLib`) and re-do Part (4). **Deliverables for this item: [10 points] Annotate your schematic from Part (4) and add BLUE arrows representing the direction of small-signal current flow in each MOSFET. Again assume that the current in NM0 is the reference.**
6) Next, run an AC simulation sweeping the input frequency from 1Hz to 10GHz, what is the DC gain? Finally, what is the input capacitance to each input terminal of the differential pair? (HINT: You know the equation for the impedance of a capacitor; how can you take that and other results from your AC simulation to calculate the input capacitance?) **Deliverables for this item: [5 points] Provide a plot of your frequency sweep results, mark where the unity gain bandwidth is located and also state it in your report. Also state the near near DC gain. [5 points] State what the input capacitance is for each input terminal of the differential pair. Also, show your calculations and explain how you obtained your answer.**
7) **Final deliverables for Part 1: [10 points] Calculate the output resistance of the differential pair (Hint: you can use values for g_{ds} found in the detailed DC bias output, using the Results Browser from the ADE menu). What is the output resistance? What is the small signal gain, using $A_v \approx g_m\ (r_{o2}||r_{o4})$? Compare this to the differential gain found above. Are they the same? Why or why not? [10 points] Now, find out the output resistance by obtaining relevant values through simulation! This can be done by adding a test source the the output of the circuit (VDC) and a load resistor (1kΩ) in series with it, take the voltage at the output node AFTER the resistor and find the resulting current, and from that calculate the output resistance. How does it match up with your previous value?**

III. Differential Pair Improvement

This section is worth 30% of the lab value. Each question posed below is equal value.

A. CMR Improvement

You are required to **widen the CMR of the differential pair**. Change one or more parameters (MOSFET width, MOSFET length, bias point, but NOT voltage supply) to achieve this goal. **Explain what you did and why, and provide proof that your modification worked.** Complete schematics and all device sizes must be included, showing clearly any values that have been modified.

B. Gain Improvement

You are required to **increase the differential gain** of the differential pair (this question is independent of the previous question). Change one or more parameters (MOSFET width, MOSFET length, bias point, but NOT voltage supply) to achieve this goal. **Explain what you did and why, and provide proof that your modification worked.** Complete schematics and all device sizes must be included, showing clearly any values that have been modified.