UNIVERSITY OF LIVERPOOL

Department of Electrical Engineering and Electronics

ELEC473

Digital Systems Design
Assignment 1
Serial Communications

Module	ELEC473
Coursework name	Assignment 1
Component weight	15%
Semester	1
HE Level	7
Lab location	PC labs 301, 304 as timetabled, at other times for private study
Work	Individually
Timetabled time	12 hours (3 hours per week – Tuesdays 1pm – 4pm)
Suggested private study	10 hours including report writing
Assessment method	Individual, formal word-processed reports (Block diagrams and ASMs can be hand drawn and scanned into the report)
Submission format	Online via CANVAS
Submission deadline	23:59 on Sunday 26th November 2023
Late submission	Standard university penalty applies
Resit opportunity	Students Failing Assignment 1 will have Assignment 2 as the resit opportunity. Students Failing the module and Assignment 2 will have an alternative assignment in the Summer
Marking policy	Marked and moderated independently
Anonymous marking	Yes
Feedback	Via comments on CANVAS
Learning outcomes	LO1: Ability to design digital systems using the ASM design method LO2: Ability to implement digital systems using the Verilog Hardware Description Language

Marking Criteria

Section	Marks available	Indicative characteristics	
		Adequate / pass (50%)	**Very good / Excellent**
Presentation and structure	20%	• Contains cover page information, table of contents, sections with appropriate headings. • Comprehensible language; punctuation, grammar and spelling accurate. • Equations legible, numbered and presented correctly. • Appropriately formatted reference list.	• Appropriate use of technical, mathematic and academic terminology and conventions. • Word processed with consistent formatting. • Pages numbered, figures and tables captioned. • All sections clearly signposted. • Correct cross-referencing (of figures, tables, equations) and citations.
Introduction, Method and Design	40%	• Problem background introduced clearly. • Evidence of a Top Down Design approach • Conceptual Design Choices introduced. • Design of each module follows a logical sequence. • ASMs correspond to designs for each block.	• Appropriate range of references used. • Design decisions justified with alternatives given. • Calculations shown in full, justifying and explaining any decisions. • Correct ASM Syntax used. • Well-structured Verilog Code • Fully synchronous design
Results	30%	• Simulation results present for each block and well annotated. • Results of full system in both simulation and experimentally presented. • Results for each task accompanied by a commentary. • Screen shots of results presented.	• Simulations demonstrate that every pathway in each ASM is functioning correctly. • Tests indicate that there are no problems caused by asynchronous inputs.
Discussion	10%	• Discussion on what worked and what didn't. • Critical assessment on the design – strength and weaknesses	• Discussion on how the system was fully tested.

ELEC 473 Verilog Assignment 1 (2023-2024)

Assignment Overview

This assignment has been set to get you familiar with designing digital systems and synthesising them from a Verilog description. You should develop your design using Altera's Quartus II V13.0sp1 and test your design on the DE2-35 board.

Assignment Outline – Part A

The DE2 Board has a 9 pin D type connector and associated level shifting circuitry to allow the board to be connected to the RS232 port of another electronic device. Figure 1 shows the circuit on the DE2 board which includes a MAX232 device that performs the voltage conversion and also two LEDs which indicate if there is any activity on the transmit or receive signals. These LEDs are normally off and pulse when data is being transmitted.

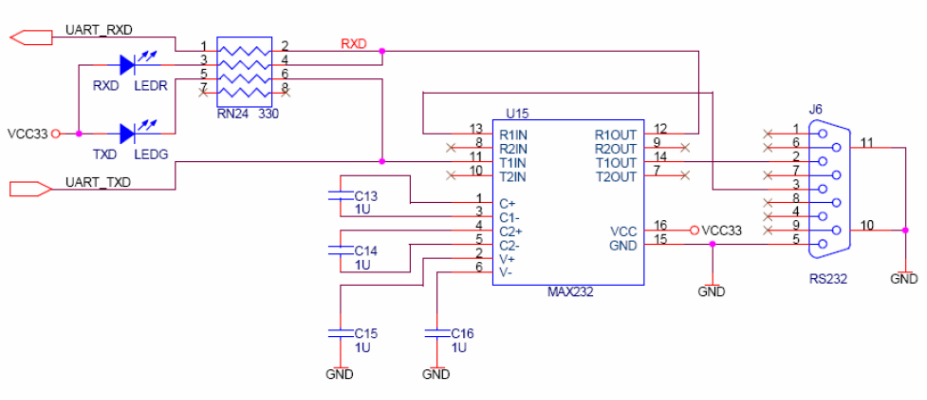

Figure 1 RS232 Level conversion circuit

Table 1 shows which pins of the FPGA are connected to the MAX232 device. Note that UART_RXD is the input received signal as received on pin 3 of the 9 pin D-Type and UART_TXD is the output transmitted signal sent to pin 2 of the 9 pin D-Type. Pin 5 carries the GND signal between the two systems.

Table 1 FPGA Pin connections

Signal Name	FPGA Pin No.	Description
UART_RXD	PIN_C25	UART Receiver
UART_TXD	PIN_B25	UART Transmitter

For this assignment you are to develop a UART transmitter to serially transmit data from the DE2 board, via the serial link, to a PC running a terminal program, for example "Putty". The PC should then display the ASCII value of the data transmitted. For example if 0x41 was transmitted a capital 'A' should be displayed. The data is entered by keying in the binary data on the "inputs" and then transmitted when the "send" key is pressed. The data should be transmitted with the baud, parity and number of bits indicated in Table 2 and also displayed on the displays indicated in Table 2. You should use Key[0] as a system reset, note that the Keys are active low i.e. normally high but going low when pressed.

Make sure that your design is fully synchronous, i.e. all the D type flip-flops should be clocked by the 50 MHz system clock.

Your "top level" Quartus file can be either a "bdf" or Verilog file.

Note that more modern PCs do not have a built in serial port on the Motherboard, so you will need to use a USB to RS232 adapter cable available from the technician. To see what communications port it gets mapped to, use "Device Manager" in Windows and then look at the "Ports (COM &LPT)" to see what COM port it is mapped to (it will probably be COM 4).

Reports

Your report should include the following.

1) Description of Architecture(s) and Controller(s) (with block diagram showing interconnections). (Maximum 2 pages A4)
2) Description of each module to be documented by the following information
    a. ASM Charts for any Algorithmic State Machines and any combinational logic (Remember Combinational Logic can be treated as a single state ASM).
    b. Commented Verilog code for each module.
    c. Full simulation of each module. (With annotations indicating what the simulation proves).

    This information should be grouped together for each module i.e. there should be a single section covering the above for each module. (Don't group all the ASMs together, the marker needs to be able to linearly read through the report without flipping forwards and backwards. They first want to see the ASM, then the Verilog, then the simulation for each block).
3) Schematic of the full system if a "bdf" is used otherwise the Verilog of the full system.
4) Simulation of the full system. (With annotations and maximum ½ page on any comments)
5) Explanation of experimental test results. (Max 1 page)
6) Conclusion/Discussion (Maximum ½ page)
7) You should also submit your design via CANVAS as a ZIP file. Make sure all the files need to compile simulate and test the design are included.

Please format your report in the order indicated above, i.e. fully document each module before describing the next module.

Warning

When marking the reports I will be looking very closely for any signs of collusion, as this is unacceptable. I need to assess your own ability not that of your friend or colleague. If I find any evidence of collusion then the University's rules on the punishment for collusion will be followed. If you do collude I will spot it and you will be penalised – you have been warned.

Submission Deadline

Demonstration: Tuesday 21st November 2023
Electronic copy: Sunday 26th November 2023 @ 11:59pm on CANVAS

J.S.Smith (24/10/2023)

Notes:

1. When you have finished Assignment 1 you can start on Assignment 2 which will be to implement a full UART i.e. to add a receiver to your transmitter, which will display the received value on some other 7 segment displays. For Assignment 2 you will have a mode switch to switch between RS232 and IrDA communications.
2. Whilst the boards have been serviced, some may still have intermittent "Keys". It is advised to connect Key[0]-Key[3] to LEDG[0]-LEDG[3] so that you can check that contact has been made when the switch is pressed.
3. Design using small simple modules that can be re-used, for example the same shift register design could be use in the receivers as well as the transmitter if you plan in advance.
4. Block diagrams and ASM can be hand drawn and then scanned into the report, there is no need to use a drawing package

Table 2 – Assignment parameters

ID	Student Name	Baud Rate	Parity	Data Bits	Inputs	Send	Outputs
2015353	Abrams, James Nguyen	9600	Odd	7	Sw[6:0]	Key1	Hex7-6
2013559	Amu, Evelyn Emefa	19200	Odd	7	Sw[7:1]	Key2	Hex6-5
2014073	Butt, Adam	38400	Odd	7	Sw[8:2]	Key3	Hex5-4
2017596	Cao, Morty	57600	Even	7	Sw[9:3]	Key1	Hex4-3
2016088	Chapman, Kathryn Julia	9600	Even	7	Sw[11:5]	Key2	Hex2-1
2016973	Chen, Xingyu	19200	Even	7	Sw[12:6]	Key3	Hex1-0
2017658	Dsouza, Rupal	38400	Odd	7	Sw[13:7]	Key1	Hex7-6
2017507	Hanumaiah Gowda,	57600	Odd	8	Sw[14:7]	Key2	Hex6-5
2017166	He, Wanli	9600	Odd	8	Sw[15:8]	Key3	Hex5-4
2017094	Jiang, Xu	19200	Even	8	Sw[17:10]	Key1	Hex4-3
2016697	Keerthi, venkat	38400	Even	8	Sw[9:2]	Key2	Hex2-1
2013969	Marshall, Amy Victoria	57600	Even	8	Sw[10:3]	Key3	Hex1-0
2015161	Michael Ravichandran,	9600	Odd	8	Sw[12:5]	Key1	Hex7-6
2015185	Okotobei, Wellington Jnr	19200	Odd	8	Sw[13:6]	Key2	Hex6-5
2014818	Orton, Sam	38400	Odd	7	Sw[13:7]	Key3	Hex5-4
2017742	Orugonda, Mohan	57600	Even	7	Sw[14:8]	Key1	Hex4-3
2017231	Palanisami, Nivedhitha	9600	Even	7	Sw[15:9]	Key2	Hex2-1
2017765	Parepalli, Srinivas	19200	Even	7	Sw[16:10]	Key3	Hex1-0
2017521	Patil, Nikhil	38400	Odd	7	Sw[12:6]	Key1	Hex7-6
2017654	Premakumar, Lakshmi	57600	Odd	7	Sw[13:7]	Key2	Hex6-5
2015107	Ross, Jamie	9600	Odd	8	Sw[15:8]	Key3	Hex5-4
2013823	Shipilov, Dmitry	19200	Even	8	Sw[17:10]	Key1	Hex4-3
2017526	Siddiqui, Saad	38400	Even	8	Sw[9:2]	Key2	Hex2-1
2014611	Stoian, Geanina Nicoleta	57600	Even	8	Sw[10:3]	Key3	Hex1-0
2017009	Sundararajan, Anjan	9600	Odd	8	Sw[12:5]	Key1	Hex7-6
2017504	Thaipakdee, Khanthapak	19200	Odd	8	Sw[13:6]	Key2	Hex6-5
2017491	Topcu, Kemal	38400	Odd	8	Sw[15:8]	Key3	Hex5-4
2017533	Vorsu, Rohith	57600	Even	7	Sw[6:0]	Key1	Hex4-3
2017657	Wenyu, Ma	9600	Even	7	Sw[7:1]	Key2	Hex2-1
2017081	Zhou, Siwei	19200	Even	7	Sw[8:2]	Key3	Hex1-0