2023-24

Assignment-II

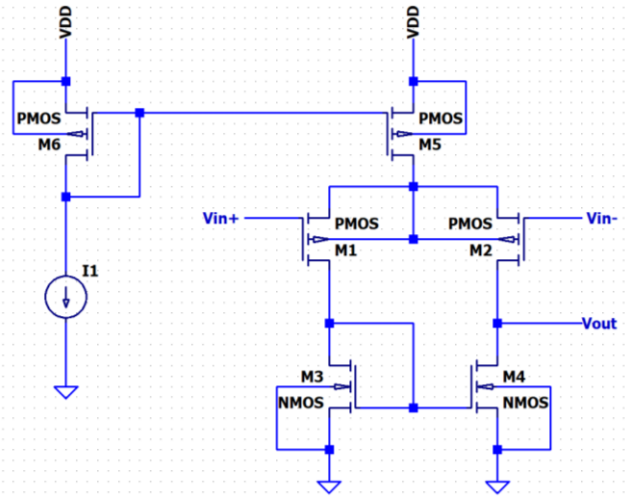
VLSI Design & Technology (ELC3611)

Max. Marks = 5 [CO4] **Due Date for Submission: October 31, 2023**

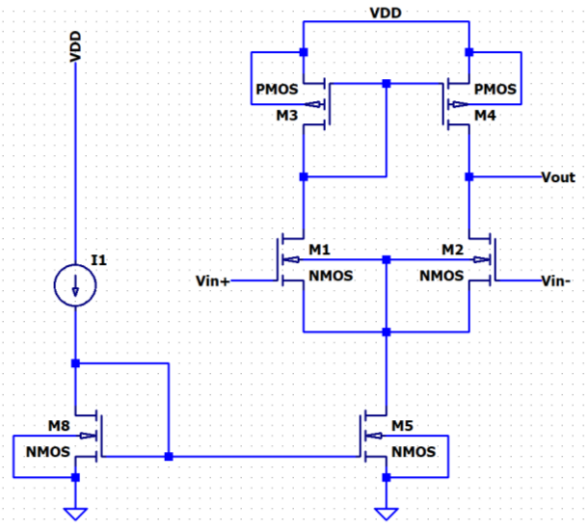
Design a one stage Op-Amp that satisfies following specifications:

Power Dissipation ≤ (<last three digits of your faculty no> * 4) µW
-3dB frequency ≥ (<last three digits of your faculty no> * 11.78) kHz for C_L = 5 pF
Low frequency voltage gain (A_V) = 30 ±10%
$V_{out(dc)}$ = Vdd/3 for topology (a)
2Vdd/3 for topology (b)

Important: Students with even (odd) serial no. shall use PMOS (NMOS) driver and NMOS (PMOS) current mirror load



(a) Topology for even sr. no. students



(b) Topology for odd sr. no. students

Use the attached model file cmos180.txt

You shall upload your LTSPICE file here on google classroom and submit a hardcopy of the Assignment Report consisting of the following:

1. Design approach/steps
2. Neat circuit schematic with L and W of transistors appended
3. Transient analysis waveform
4. Frequency response
5. Summary Table of the performance metrics

FoM	Given Specification	Pre-layout Simulation Results
Power Dissipation		
Gain		
-3dB Bandwidth (MHz)		
Unity Gain Bandwidth	Not specified	
Output Impedance	Not specified	
Slew Rate	Not specified	
ICMR	Not specified	
Output Swing	Not specified	
CMRR	Not specified	
PSRR	Not specified	

6. Layout of the core (M1 – M5) of the circuit topology