PERVASIVE CARDIOVASCULAR AND RESPIRATORY MONITORING DEVICES

Chapter 4 Electronics

ABSTRACT

This chapter describes electronic components used in biomedical devices, including operational amplifiers, filters, analog to digital and digital to analog converters, and others. The goal is to show how to connect transducers with the digital system using conditioning or interfacing circuits. Different amplifiers are presented, including differential, instrumentation, programmable-gain, transimpedance, and charge amplifiers. It is important to understand what type of amplifier should be used with what transducer or sensor. In addition, we explain the effect of filtering and aliasing on the signal. All the components are simulated, and simulation results are presented. We also describe performance metrics used to quantify the performance or errors of different components. New developments in the field, including state-of-the-art integrated solutions that include many analog components in a single chip, will also be presented.

Keywords: Operational amplifiers, Filters, A/D converters, D/A converters, signal generators, pulse width modulation, Wheatstone bridge, differential amplifier, instrumentation amplifier, programmable-gain amplifier, transimpedance amplifier, charge amplifier, Sallen-Key filter, sampling, aliasing, quantization, pulse width modulation.

CONTENT

4.1. Introduction

This chapter focuses on biomedical system components for signal conditioning and conversion to digital signals. The majority of biomedical devices nowadays are designed similarly to the system shown in Fig 1.2. Transducers have been introduced in the previous chapter. This chapter presents analog processing components, including conditioning circuits, amplifiers, and filters. They are presented in blue in Fig 1.2. Filters remove undesired frequency components of the signal. In a system where processing is done in software, the signal is filtered using an antialiasing analog filter and then converted into a digital signal using an A/D converter. After that, the signal is processed in real-time or stored and processed offline by a processor. The digital component in Fig 1.2 is signal processing and control block.

Table 4.1 shows the conditioning circuits commonly connected to the transducers that we covered in Chapter 3. For example, the resistive displacement transducers are typically connected to a Wheatstone bridge which is further connected to a differential or instrumentation amplifier. In addition to traditional conditioning circuits, we also show some modern industrial integrated solutions that connect transducers directly to the A/D converter or the microcontroller.

In this chapter, we first start with bridge circuits. Next, we introduce operational amplifiers and show their different configurations. Then, we present different conditioning circuits based on operational amplifiers for connecting electrodes (instrumentation amplifiers), piezoelectric transducers (charge amplifiers), and capacitive transducers (synchronous demodulation). Also, we show some operational amplifier solutions for linearizing the bridge circuits. Next, we present passive and active filters. After that, we introduced analog to digital (A/D) converters. We introduce concepts of sampling, aliasing, errors

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during the conversion and other concepts needed to understand the functioning of A/D converters. We then show several integrated special-purpose configurations of converters, including capacitance to digital converters, time to digital converters, and others. Components used for generating signals are covered next, including digital to analog (D/A) converters and pulse width modulation (PWM) circuits. Integrated special-purpose D/A converters and PWM circuits are discussed as well.

Table 4.1 Transducers and their conditioning circuits

Transducer	Conditioning circuit	Integrated circuit with the conditioning circuit and other components
Strain gauges	Wheatstone bridge and a differential amplifier	Bridge transducer A/D converter
Piezoelectric	Charge amplifier	Integrated solution that include charge amplifier
Capacitive	AC bridge, synchronous demodulation	Capacitance to digital converter
Photodiodes	Transimpedance amplifier	Current to digital converters, current to frequency converters
Electrodes	Instrumentation amplifier	ECG integrated circuits

Acronyms and explanations

GBWP	gain bandwidth product
CMRR	common mode rejection ratio
CMG	common mode gain
LSB	least significant bit
PGA	programmable gain amplifiers
SPI	Serial Peripheral Interface
I^2C	Inter-Integrated Circuit
ADC	analog to digital converter
DAC	digital to analog converter
CDC	capacitance to digital converter
PGA	programmable gain amplifier
DDS	direct digital synthesis
PWM	pulse width modulation
MCU	microcontroller
DMA	direct memory access
RAM	random access memory
MAC	multiple and add/accumulate

Variables used in this chapter include:

- N number of bits at the output of an A/D converter or the input of a D/A converter
- V_o analog output voltage
- V_{in} analog input voltage
- S sensitivity
- A gain of an operational amplifier
- A_d differential gain
- A_c common mode gain
- τ time constant
- f_c cut-off frequency
- T signal period and PWM period
- T_s sampling period
- f_s sampling frequency
- f_h Nyquist frequency
- V_{FS} full-scale voltage of A/D and D/A converters
- W binary code word that represents the digital input to a D/A converter
- D pulse width offset for PWM

4.2. Wheatstone bridge

Several transducers, such as temperature transducers and strain gauges, convert a physical signal into resistance. There are technical limitations that need to be addressed when using these transducers, including the accurate measurement of small resistance changes, commonly in the order of a few percent of the nominal resistance.

The simplest way to convert a resistance change into a voltage change would be to place the transducer in a **voltage divider** circuit. However, in this case, the output voltage change is a nonlinear function of the resistance change and its baseline voltage depends on the resistance of the selected resistor and the resistance of the transducer. We will show below that the baseline voltage of a Wheatstone bridge configuration has a baseline voltage of zero.

The **Wheatstone bridge** is commonly used for measuring small changes in resistance. The circuit is shown in Fig. 4.1a). It consists of four resistors connected as two voltage dividers, a voltage or current source connected across one diagonal. In our case, the bridge is excited using a voltage source V_E. The output voltage is measured across the other diagonal. Namely, the voltage difference V_o between the outputs of the voltage divider on the left (resistors R_1 and R_2) and the voltage divider on the right (resistors R_3 and R_4) is measured. The output voltage V_o is a of the change in the resistance:

$$V_O = V_E\left[\frac{R_1}{R_1+R_2} - \frac{R_3}{R_3+R_4}\right] \tag{4.1}$$

When $V_o = 0$ the bridge is balanced, meaning that $R_1/R_2 = R_3/R_4$. The voltage V_o is then amplified using an amplifier that we will introduce later in the chapter. The bridge with only one transducer is called the quarter bridge or the single-element varying bridge. The quarter bridge is suited for temperature sensing and for applications with a single resistive strain gauge. Let us assume that the transducer is placed in the bridge in the right leg and that its resistance is R_3. Further, let us assume that $R_1 = R_2 = R_4 = R$ and that the transducer resistance can be represented as $R_3 = R + \Delta R$ where ΔR represents changes in the resistance which can be, in general, both positive and negative. R is the nominal resistance of the transducer.

The **sensitivity** of the bridge is defined as the change in the output V_o over the change of the resistance of the transducer at the input ΔR. Sometimes, the sensitivity is defined as the ratio of the maximum expected change in the output voltage to the excitation voltage, but we will use the first definition here. Based on (4.1) and by replacing the values of all resistors with R and the transducer resistance with $R_3 = R + \Delta R$, we get for V_O:

$$V_o = \frac{-\Delta R}{2(2R+\Delta R)}V_E$$

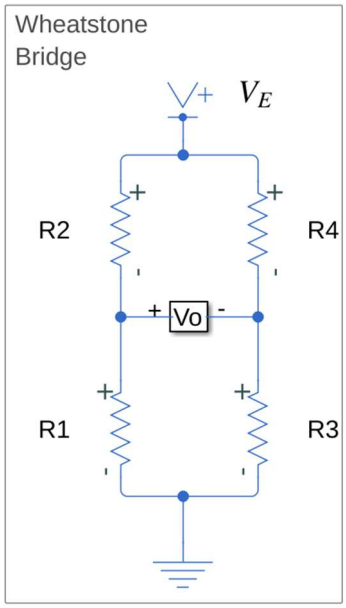
If ΔR is very small, then the sensitivity of the bridge can be approximated as

$$S = \frac{V_o}{\Delta R} = -\frac{V_E}{4R}$$

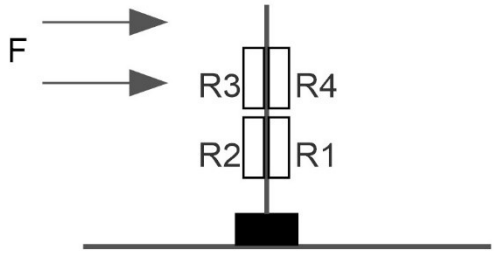
If it is possible to use two or four transducers in the bridge configured so that the resistances of half of them reduce while the resistances of another half of the transducers increase after applying the force, then the sensitivity can be improved. In addition, for four transducer configuration, the relationship between V_O and ΔR is linear:

$$V_O = \frac{\Delta R}{R_o}V_E$$

Four transducer configuration is called a full bridge or all-element varying bridge. The full bridge is an industry-standard configuration for load cells based on four identical strain gauges. An example of placing four transducers on a bending vane or a beam and their organization in the bridge is shown in Fig. 4.1b). The vane or the beam will bend due to the applied force F so that the resistance R_2 and R_3 will increase while the resistances R_1 and R_4 will decrease.



a)



b)

Fig. 4.1 a) Wheatstone bridge, b) Possible full bridge configuration of strain gauges on a bending vane

If it is impossible to use four transducers, we can linearize the bridge using an operational amplifier shown in Section 4.3.6.1. AC or capacitive bridges will also be introduced in Section 4.3.6.2.

Important aspects in designing the bridge circuit include selecting a configuration with 1, 2 or 4 transducers, techniques for linearizing the bridge if necessary, selecting the excitation (current or voltage, AC or DC) and the amplifier at the output of the bridge. Other design decisions include the tolerance of resistors, on-chip or discrete bridge solution, stability of the excitation, and so on.

4.3. Amplifiers and their configurations

4.3.1 Operational amplifier

An operational amplifier amplifies the voltage difference between its inputs. They are characterized using several parameters such as:

- **Open-loop gain** A can be in the order of a million
- The relationship between the input (V_{in}^+, V_{in}^-) and the output V_o voltages is $V_o = A(V_{in}^+ - V_{in}^-)$
- **Input resistance**, R_{in} that should be very high, for example, in the order of GΩ
- **Output resistance**, R_{out} that is low in the order of 100 Ω
- Minimum and maximum output voltages that depend on the applied supply voltage
- Maximum **slew rate**, which is defined as the maximum positive or negative rate of change of the magnitude of output voltage. A typical value is, for example, 2 V/µs.
- **Open-loop bandwidth** is the frequency at which the magnitude of the frequency response drops by 3 dB compared to the magnitude at low frequencies.

An equivalent circuit of a band-limited operational amplifier is shown in Fig. 4.2a). The model describes the effects of the input and output impedance and the limited bandwidth but does not include nonlinear effects such as the slew rate. The input resistance R_{in} connected to the voltage-controlled voltage source that acts as an ideal amplifier and amplifies the input by the gain A. In this example, the gain is 100,000. A voltage-controlled voltage source maintains the output voltage proportional to the input voltage. An ideal operational amplifier is a voltage source dependent on the voltage between its input terminals. Components R_p and C_p emulate the first order lowpass filter with a cutoff frequency $1/(2\pi R_p C_p)$ that determines the open-loop bandwidth. The second voltage-controlled voltage source is set to a gain of one, and it is there to separate the input from the output. The magnitude and phase response of the equivalent circuit model of the operational amplifier is shown in Fig. 4.2a). The magnitude is 100 dB (100,000 gain) at low

frequencies, and the cutoff frequency is 1 kHz ($1/2\pi R_p C_p$). The phase response is zero degrees at low frequencies.

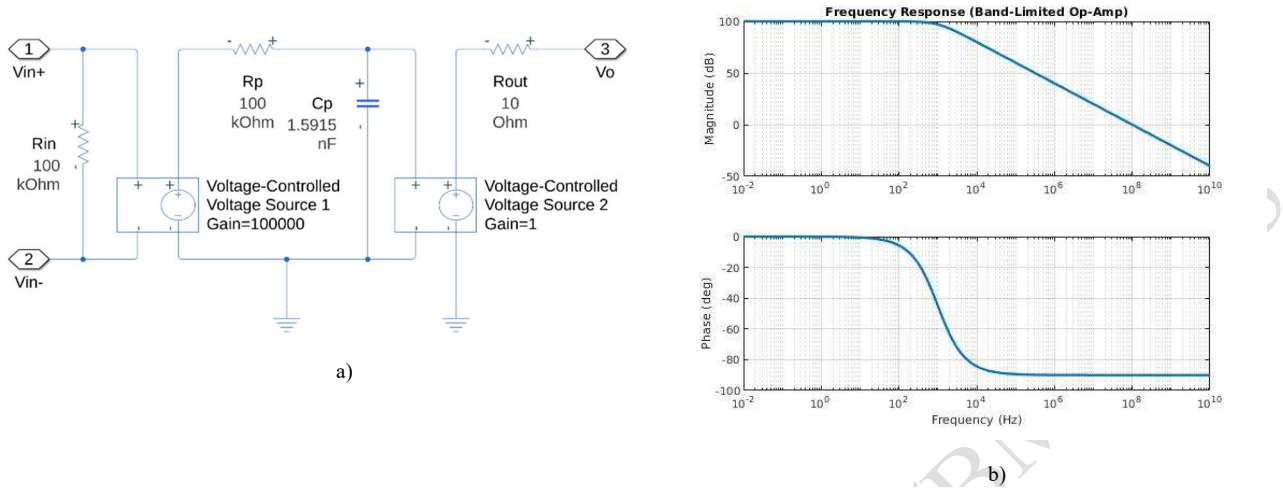


Fig. 4.2 a) The equivalent circuit of a band-limited operational amplifier, and b) its magnitude and phase response

4.3.2 Operational amplifier parameters

We will introduce several additional parameters of the operational amplifiers.

The **offset voltage** is a differential voltage that needs to be applied at the input to obtain $V_o = 0\ V$. Ideally, it should be zero. The low offset voltage that is common nowadays in precision low noise amplifiers is, for example, 10 μV. An offset trim pin is commonly provided to help remove the offset externally.

An ideal operational amplifier will have zero current at its input terminals. An **input bias current** is an input current to the realistic operational amplifier and can be modeled as two current sources connected directly to the inputs V_{in}^+ and V_{in}^- in Fig. 4.2a). For example, 20 nA bias current is common. Bias currents on both input terminals should be equal. However, in realistic operational amplifiers, there is a difference in the bias currents between the input terminals, and the absolute value of the current difference is called the **input offset current**.

The noise of the amplifier can be modeled as a voltage source connected in series to one of the inputs of the operational amplifier. Therefore, it can be considered as an offset that changes over time. In low noise amplifiers, noise can be as low as 3 nV/ √ Hz (read as 3 nanoVolts per root Hertz).

Operational amplifiers are normally used in **negative feedback configuration** in which the output is connected to one input through a **feedback circuit**. By doing that, the ideal operational amplifier will adjust the output until the difference of the voltages at the input is close to zero. When used as amplifiers, several more performance metrics play important roles. One is **Gain BandWidth Product** (GBWP) which represents a product of the open loop gain and the open-loop bandwidth. However, GBWP remains constant as the gain of the operational amplifier in the closed-loop decreases, the cut-off frequency of the operational amplifier increases. For example, from the magnitude response in Fig. 4.2b), we can see that the frequency is 100 MHz when the gain is 1 (magnitude is 0 dB), and therefore, GBWP=100 MHz.

In operational amplifiers, if the voltage at both inputs is equal, the voltage at the output should be zero. This voltage is called **common mode voltage** and usually appears as interference at the inputs of the operational amplifiers. In realistic operational amplifiers, the output is not zero where the is a common mode voltage. The finite attenuation of the common mode voltage is called **common mode gain** (CMG) – we will use a symbol A_c for CMG. A **common mode rejection ratio** CMRR is an important characteristic of operational amplifiers that is defined as the ratio of the differential gain versus the common mode gain. It is commonly given in decibels. CMRR can be quite large, commonly more than 100 dB. It drops with increasing frequency.

4.3.2.1 Operational amplifier supply voltage

Double supply or dual voltage operational amplifiers have positive (V_{cc}) and negative ($-V_{cc}$) voltage supplies. The rail refers to the supply voltage levels. **Rail-to-rail** double supply operational amplifier is the amplifier whose output voltage can swing from $-V_{cc}$ to V_{cc}.

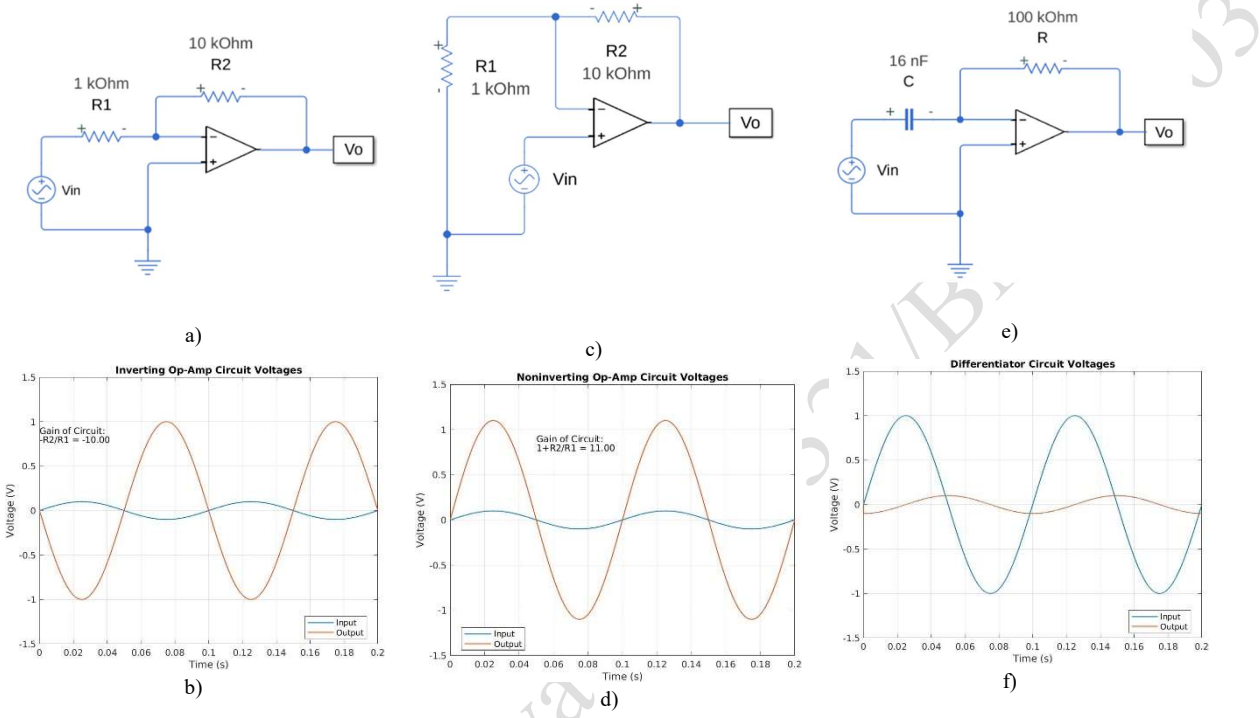
A **single supply** operational amplifier requires only one voltage supply (V_{cc}) and therefore, the upper rail is V_{cc} and the lower rail is the ground. Rail-to-rail single supply operational amplifier is the amplifier whose output voltage can swing from 0 to V_{cc}.

Many amplifiers are not rail-to-rail because the output voltage of the amplifier cannot reach the supply voltage. The difference between the supply voltage and the maximum voltage of the operational amplifier is sometimes called the headroom.

Single supply operational amplifiers are more prevalent nowadays in battery-operated biomedical devices.

4.3.3 Processing circuits

Many analog processing circuits can be built based on operational amplifiers. They include inverting and non-inverting amplifiers, adders, multipliers, differentiators, integrators and so on. Special purpose circuits, such as amplifiers with differential inputs and active filters, will be explained Sections 4.3.4 and 4.4. -Fig. 4.3 shows the circuits and the signals of inverting, noninverting and differentiator operational amplifier circuits. The input signal for all three circuits is sinewave with an amplitude of 1 V and at frequency of 1 Hz. The noninverting amplifier does not change the phase of the input signal. The inverting amplifier changes the phase by 180º while the differentiator changes the phase by 90º.



-Fig. 4.3 Three amplifier configurations and their signals at the input and the output: a, b) Inverting amplifier, c, d) Noninverting amplifier and e, f) Differentiator.

The gain of the **inverting amplifier** is $V_o/V_{in} = -R_2/R_1$. Therefore, in the circuit in -Fig. 4.3a), the gain is -10.
The gain of the **noninverting amplifier** is $V_o/V_{in} = 1 + R_2/R_1$. Therefore, in the circuit in -Fig. 4.3c), the gain is 11.

Let us derive the relationship between the input and the output for the **differentiator**. The current i through the resistor R is equal to the current through the capacitor if the operational amplifier is ideal:

$$i = -\frac{V_o}{R} = C \cdot \frac{dV_{in}}{dt}$$

The output voltage is then:

$$V_o = -RC \cdot dV_{in}/dt$$

The amplitude response can be computed in the frequency domain by applying Fourier transform. Therefore:

$$|V_o\ (j\omega)/V_{in}\ (j\omega)| = \omega RC$$

where ω is the angular frequency $\omega = 2\pi f$.

The differentiator is actually an active highpass filter. The problem with the differentiator implemented in this way is that it might become unstable at high frequencies and is sensitive to noise. Practical implementation of the differentiator usually involves the addition of a small capacitance in parallel with the resistor R as well as the addition of a resistor connected in series with the capacitor C. The additional capacitor prevents the circuit from becoming unstable at high frequencies, while the additional resistor will limit the increase in gain with frequency (please observe that the gain keeps increasing with frequency in the original differentiator implementation). For more details, please consult [Northrop14], [Webster10].

The integrator circuit is shown in Problem 4.19 and the computation of its gain is given as an exercise for the readers.

4.3.4 Differential amplifier

The differential amplifier is shown in Fig. 4.4. The differential amplifier amplifies the difference between the input signals. Therefore, the output is computed as $V_O = A_d(V_2 - V_1)$ where A_d is the differential gain of the differential amplifier.

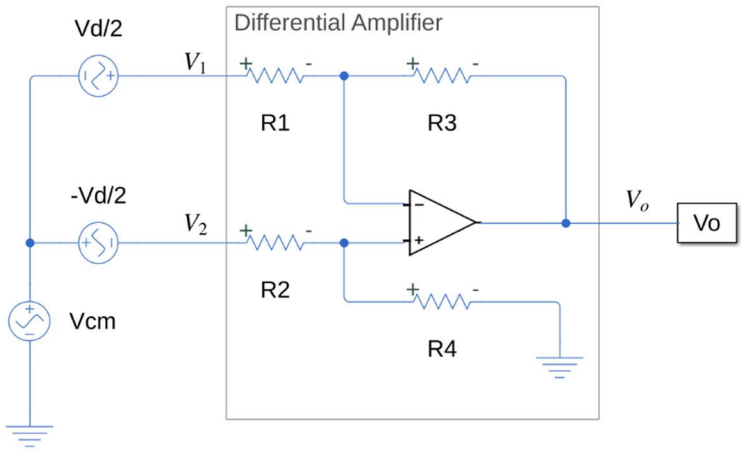


Fig. 4.4 Differential amplifier

The amplifier is extremely sensitive to the imbalance of the resistor values, and therefore, it is critical to satisfy the following condition: $R_3/R_1 = R_4/R_2$. Consider the differential amplifier in Fig. 4.4, and let us assume that $R_1 = R_2$ and $R_3 = R_4$. The output of the amplifier is:

$$V_O = \frac{R_3}{R_1}\left(\frac{1 + R_1/R_3}{1 + R_2/R_4}V_2 - V_1\right) \tag{4.2}$$

$$V_O = \frac{R_3}{R_1}(V_2 - V_1) \tag{4.3}$$

This mean that the amplifier really works as a differential amplifier and that the differential gain is determined by the selection of resistors R_3 and R_1 and its value is $A_d = R_3/R_1$. CMG is zero in this case, and therefore, CMRR is infinite. In practice, differential amplifiers have high CMRR, but not infinite, due to mismatch of the resistors and other imperfections of the circuit.

4.3.4.1 CMRR of a differential amplifier

We defined CMRR in Section 4.3.2. In this section, we will show the effect of common mode rejection for differential amplifiers and derive CMRR for the case when one resistor has a higher tolerance than the others.

The output voltage of the differential amplifier V_o can be written as a sum of contributions from differential and common mode inputs:

$$V_o = A_d V_d + A_c V_{cm}$$

Next, differential voltage and common mode voltage can be written as:

$$V_d = V_2 - V_1$$

$$V_{cm} = (V_2 + V_1)/2$$

CMRR is defined as: $CMRR = A_d/A_c$

Example 4.1 The amplifier has a differential gain $A_d = 1000$ and common mode gain $A_c = 0.003$. Let us assume that the signal of interest is a cardiac signal modeled as a sinewave with a frequency of 1.2 Hz and that the interference is a 60 Hz sinewave signal. The amplitude of the interference signal is assumed to be much larger than the amplitude of the cardiac signal. Also, assume that the signal of interest is differential and that the interference is the common-mode voltage. The signal at the input of the differential amplifier is:

$$V_2 = 0.02\sin(1.2 \cdot 2\pi t) + \sin(60 \cdot 2\pi t)$$
$$V_1 = -0.02\sin(1.2 \cdot 2\pi t) + \sin(60 \cdot 2\pi t)$$

a) What is the CMRR of this amplifier?

Find the signal-to-noise ratio:

b) at the input, and

c) at the output.

Solution:

a) CMRR=1000/0.003=333,333. It is common to present CMRR in decibels. Therefore, $CMRR = 20 \cdot log(A_d/A_c) = 110.5\ dB$, where log is the base 10 logarithm.

Signal to noise ratio is defined as $SNR = 20log(V_{signal}/V_{noise})$, where V_{signal} represents the amplitude of the signal, and V_{noise} is the amplitude of the noise.

b) The amplitude of the signal of interest is 0.04 V, while the amplitude of the interference is 1 V. Therefore, $SNR_{in} = 20log(0.04/1) = -28\ dB$.

c) At the output, the signal and the noise are multiplied by the differential and common mode gain and, therefore

$$SNR_{out} = 20log((0.04 \cdot 1000)/(1 \cdot 0.003)) = 82.5\ dB$$

Therefore, we can see that the signal-to-noise ratio from the input to the output is improved by $82.5\ dB - (-28dB) = 110.5\ dB$, which is exactly the CMRR of this differential amplifier.

Now, let us assume that $R_1 = R_2$ and $R_3 = R_4$ and that the tolerances of R_1, R_2 and R_4 resistors are negligible, while the R_3 resistor's tolerance is $er = 0.5\%$ (mismatch of 1%) and it is presented as $R_3(1 - er)$. The common-mode voltage is no longer zero for this differential amplifier. To calculate the CMG, we will assume that $V_1 = V_2 = V_{cm}$ and plug these values into (4.2).

$$V_O = \frac{R_3 er}{R_1 + R_3} V_{cm}$$

However, the 0.5% error barely influences the differential gain. Therefore, the CMRR will be very much dependent on the CMG:

$$CMRR = \frac{A_d}{\frac{R_3 er}{R_1 + R_3}}$$

Table 4.2 Effect of resistor accuracy on CMRR and differential gain. Please note $CMRR = -CMG$ in decibels since $A_d = 1$.

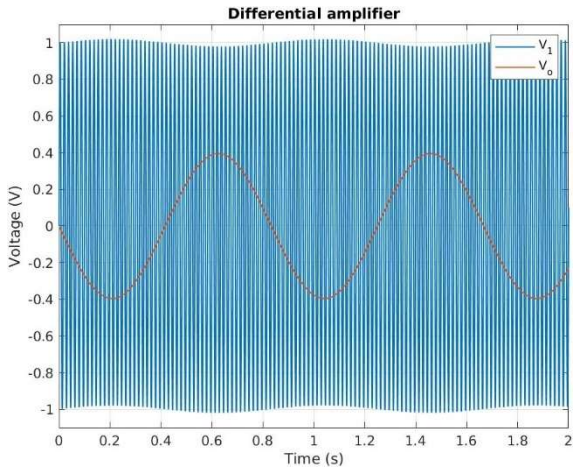
Resistor error (R_3)	CMRR
1%	46db
0.1%	66db
0.01%	86db

Table 4.2 shows the CMRR when $A_d = 1$ ($R_1 = R_3$). CMRR is low if the error is 1%. For the error of 0.01% , the CMRR is 86db, which is acceptable for most applications.

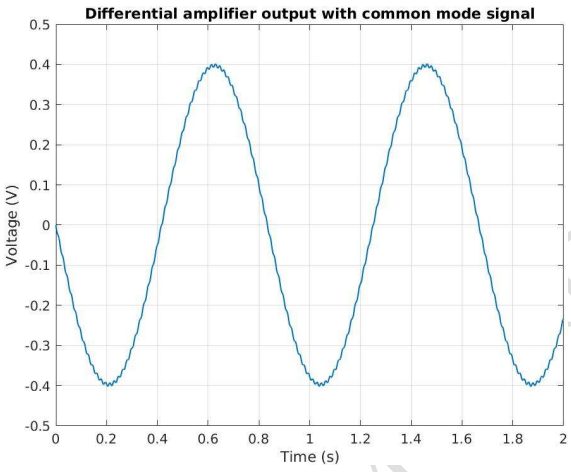
Several problems have been identified when using the differential amplifier, including:

- The input impedance is limited and depends on selected resistors.
- The differential gain is dependent on a good match of the resistors $R_3/R_1 = R_4/R_2$.
- CMRR drops significantly with increasing the tolerance in the resistor R_3.

Next, we will consider the signal at the input and the output of the differential amplifier in cases a) when all resistors are perfectly matched and have zero percent tolerance, and b) when the resistor R_3 has 1% tolerance. We use the differential amplifier shown in Fig. 4.4 and the resistors are selected so that A_d=10. The signals V_1 and V_2 are the same as in Example 4.1. In Fig. 4.5a), we show the input signal V_1 and the output signal V_o. We can see that, at the input, the common mode signal is dominant. However, since the differential amplifier is ideal, the common-mode signal is completely removed, and the output is the 10 times multiplied differential input. In Fig. 4.5b), the common-mode signal is not completely removed but is significantly attenuated. The CMG is -46 dB, based on Table 4.2. Therefore, the common mode signal still appears as noise over the amplified differential signal.



a)



b)

Fig. 4.5 a) The input and the output signal of an amplifier shown in Fig. 4.4. The input signal is given in Example 4.1. b) The output signal of an amplifier is shown in Fig. 4.4 when the value of the resistor R_3 is changed by $er = 0.5\%$.

4.3.5 Instrumentation amplifier

Some of these issues recognized by the differential amplifier are addressed by using a more advanced configuration of the differential amplifier, that is called an instrumentation amplifier. In biomedical instrumentation, it is very important that the amplifier has a large input impedance. Therefore, two voltage followers are used, and they are connected to the differential inputs. The voltage follower is a configuration with a gain of 1 and the input impedance that corresponds to the input impedance of the selected operational amplifier, which is normally very high.

The instrumentation amplifier is usually based on three operational amplifiers, as shown in Fig. 4.6. We can see that the instrumentation amplifier is composed of two voltage followers followed by the differential amplifier. We have already computed the gain of the differential amplifier in (4.2) for the case when $R_1 = R_2$ and $R_3 = R_4$: $V_O = -R_3/R_1\,(V_3 - V_4)$. Ideally the CMG=0 for the differential amplifier.

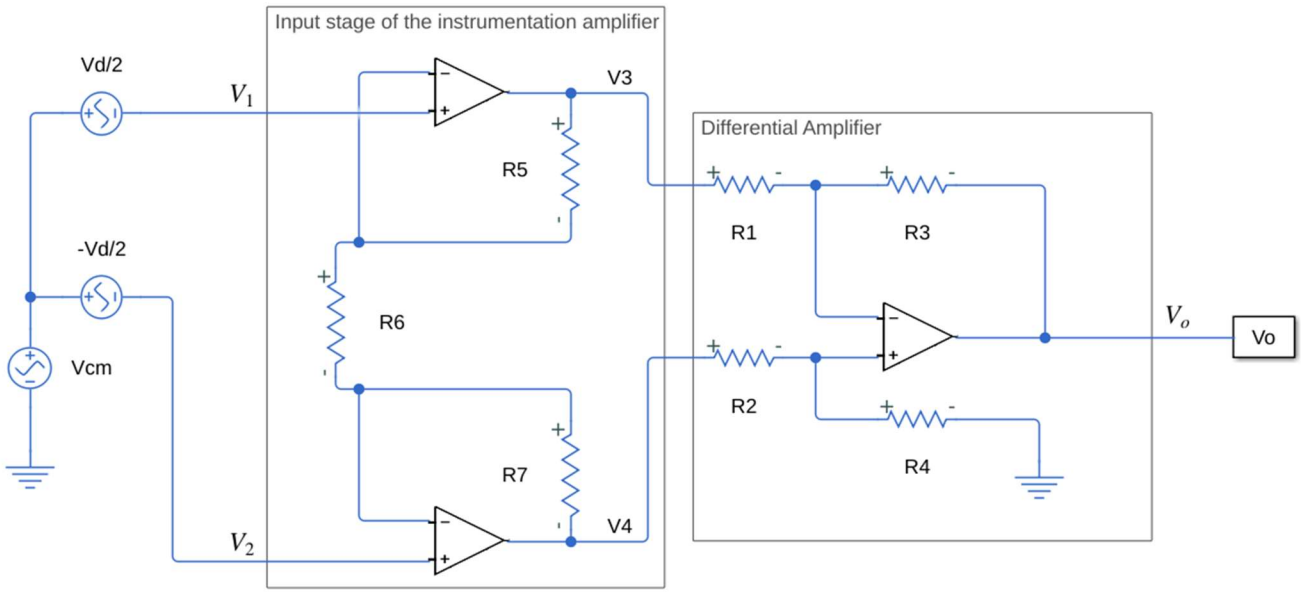


Fig. 4.6 An instrumentation amplifier

Next, we will consider the circuit on the left in Fig. 4.6. This circuit has high input impedance because the inputs are connected directly to the voltage followers. However, this configuration still has a problem: we need to address the problem of amplifying the common-mode voltage. This is achieved by adding resistors between the junctions, as shown on the left side of Fig. 4.6. R_6 is often called a gain resistor. The current i through the resistors R_5, R_6 and R_7 can be computed as

$$i = \frac{1}{R_5 + R_6 + R_7}(V_3 - V_4) = \frac{1}{R_6}(V_1 - V_2)$$

The differential gain of the left part of the circuit is then:

$$\frac{(V_3 - V_4)}{(V_1 - V_2)} = \frac{R_5 + R_6 + R_7}{R_6}$$

When $V_1 = V_2$, no current flows through R_6 and therefore $V_1 = V_3$, $V_2 = V_4$. So the common-mode gain is CMG=1.

Therefore, the differential gain of the instrumentation amplifier is

$$A_D = -\frac{R_5 + R_6 + R_7}{R_6}\frac{R_3}{R_1}$$

and the CMRR is still theoretically infinite. Please note that in Fig. 4.6, the resistor R_6 is placed on the left. When the instrumentation amplifier is implemented as an integrated circuit, it is often possible to add the resistor R_6 externally and therefore to partially control the differential gain of the instrumentation amplifier. The symbol of the instrumentation amplifier with the gain resistor is shown in Fig. 4.7.

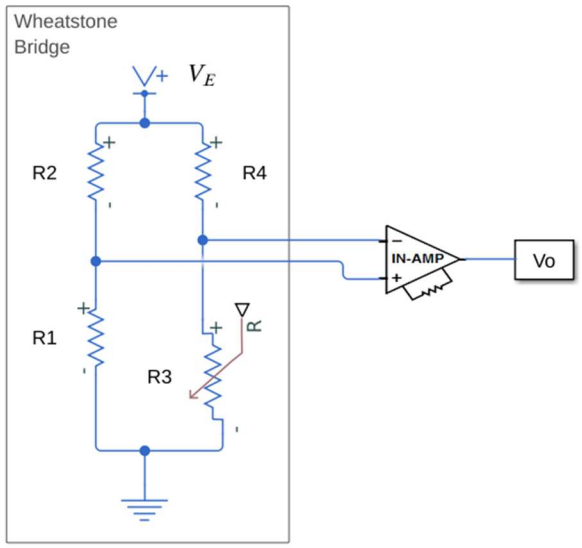
4.3.5.1 Practical considerations

Practical instrumentation amplifiers have an input impedance greater than 1 $G\Omega$, and the input bias current in the order of several nA. Gain is normally determined by attaching the gain resistor R_6 externally or by selecting or combining the internal gain resistors. A gain-programmable instrumentation amplifier can have four or more internal gains that a microcontroller can set. An example of a programmable gain amplifier with a gain of 1, 2, 4 or 8 is AD8251 by Analog Devices. CMRR is normally 90 dB to 120 dB or more in modern instrumentation amplifiers [Kitchin06].

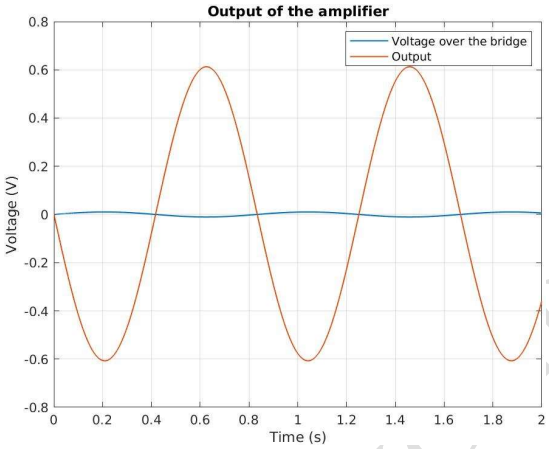
The power supply current of typical instrumentation amplifiers is of the order of 1 mA. However, micro and ultra low-power instrumentation amplifiers are used in wearable devices. An example of a low-power instrumentation amplifier is AD621, for which the power supply current is in the order of tens of μA.

Commonly, in practical applications, R_4 is not connected to the ground, but the reference voltage V_{REF} [Kitchin06]. The output voltage is measured with the reference to V_{REF}. This allows us to connect the differential input from a Wheatstone bridge that can have both positive and negative values to the instrumentation amplifier with a single supply voltage. To prevent the signal at the output of the single supply instrumentation amplifier from saturating at 0 V (having an output at 0V when the input is negative), the voltage V_{REF} has to be set properly. An example of a single rail instrumentation amplifier is AD623 by Analog Devices.

The signal output of the bridge is the differential voltage, which can be connected directly to the instrumentation amplifier's inputs. This is shown in Fig. 4.7a), where the quarter bridge is used with all resistors having a nominal resistance of 120 Ω. The resistor R_3 is a variable resistor used to simulate a transducer. The resistance of the variable resistor changes as follows: $R_3 = 120\Omega + 1\Omega \cdot sin(2\pi ft)$, where f=1.2 Hz. Fig. 4.7b) shows the signal at the output of the bridge and the signal at the output of the instrumentation amplifier that is amplified 60 times. The signal at the output of the amplifier is in the opposite phase compared to the resistance R_3. The advantage of using the instrumentation amplifier here is that the input resistance is very high and therefore does not reduce or modify the differential voltage at the input of the amplifier.



a)



b)

Fig. 4.7 a) Instrumentation amplifier connected directly to the Wheatstone bridge. b) The signal at the output of the bridge (blue line) and the signal at the output of the instrumentation amplifier (red line)

4.3.6 Using amplifiers as conditioning circuits

4.3.6.1 Linearizing Wheatstone bridge

Some transducers, such as resistive temperature transducers, cannot be connected in a full bridge. However, it is still possible to have a linear relationship between V_o and the resistance change ΔR. An example of such a system is shown in Fig. 4.8. The configuration looks like a differential amplifier. The operational amplifier used here is commonly a double supply voltage operational amplifier. In this circuit $R_1 = R_2 = R_4 = R$ and R_3 is the transducer with the resistance $R_3 = R + \Delta R$. The current i is the same through the resistors R_2 and R_4 if the operational amplifier is ideal. The relationship between the excitation V_E and the output voltage V_o can be written as:

$$V_E = V_o + (2R + \Delta R)i$$

$$V_E = 2Ri$$

By combining the two equations above, we get:

$$V_E = V_o + \frac{(2R + \Delta R)V_E}{2R}$$

Therefore, the output voltage is:

$$V_O = \frac{-\Delta R}{2R} V_E$$

We can notice that this configuration doubled the sensitivity of the quarter bridge while allowing a linear output, even for large values of ΔR.

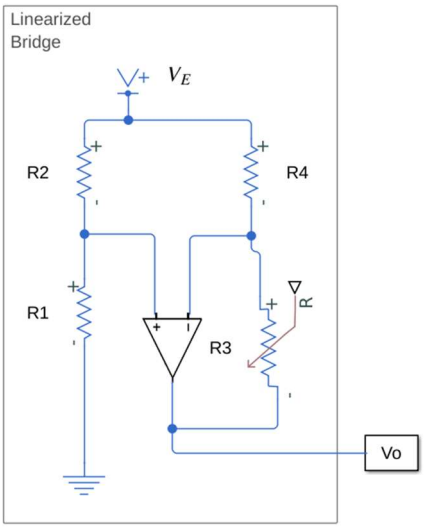


Fig. 4.8 Linear quarter bridge

Fig. 4.9a) shows the signal at the output of the bridge when the resistance of the variable resistor changes as follows: $R_3 = 120\Omega + 1\Omega \cdot sin(2\pi ft)$, where f=1.2 Hz. Fig. 4.9b) shows the relationship between the changes in the resistor value and the output voltage. We see that the change of V_o is linear with regard to the change in resistance. The curve in Fig. 4.9b) was obtained by running simulations in Simscape while linearly changing the resistance of the resistor R_3 in the range $[116.4\ \Omega, 123.6\ \Omega]$.

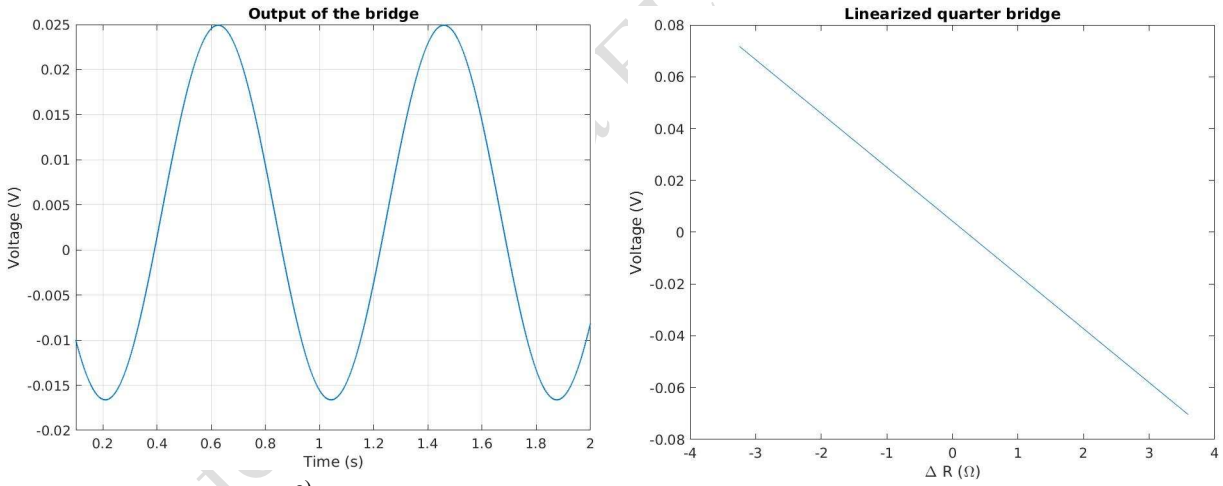


Fig. 4.9 a) The output signal of a linearized bridge. b) The linear curve shows the dependence between the change in the resistance to the output voltage change.

4.3.6.2 Interfacing capacitive sensors

Several types of interface electronic circuits were developed to connect capacitive transducers. They include ones based on resonant oscillators, AC bridges, synchronous demodulation techniques, and capacitance to digital converters [Islam17]. Capacitance to digital converters are covered in Section 4.5.4.2.

In resonant oscillators, the capacitive sensor is the part of the oscillator circuits whose frequency is inversely proportional to the capacitance. Change in the capacitance will correspond to the changes in the resonant frequency. This technique is not used much nowadays because its accuracy is affected by stray capacitance.

An AC bridge normally has one capacitive transducer C_S and a reference capacitor C on one side of the bridge and two resistors R_3, R_4 on the other side – see Fig. 4.10. It is used to detect small capacitive changes. If two capacitances are not balanced, a current will flow through the bridge. The circuit can further be linearized by using the bridge in Fig. 4.8. The output voltage is calculated as:

$$V_o = V_E\left(\frac{\frac{1}{j\omega C}}{\frac{1}{j\omega C}+\frac{1}{j\omega C_S}} - \frac{R_3}{R_3+R_4}\right) = V_E\left(\frac{1}{1+\frac{C}{C_S}} - \frac{1}{1+\frac{R_4}{R_3}}\right) \tag{4.4}$$

From (4.4), by having $R_4 = R_3$ and $C_s = C + \Delta C$ it is possible to obtain a similar relationship between changes in the capacitance and output voltage as for the standard quarter bridge. However, as we will explain later, synchronous demodulation is often used to obtain the output voltage.

A potential problem with the traditional non-linearized AC bridge is the stray capacitance between the bridge output points and the ground, and this stray capacitance can imbalance the bridge.

Next, let us consider the demodulation technique for interfacing the capacitive sensor. The capacitive sensor is coupled with a reference capacitor through a voltage divider, as shown in Fig. 4.10. Actually, an AC bridge is used with two resistors in another branch of the bridge. The capacitive sensor is modeled as a variable capacitor whose capacitance is controlled by a sinewave generator presented as the applied force block in Fig. 4.10. This bridge is connected to the input of the instrumentation amplifier, which amplifies the signal. The signal is then demodulated using a multiplier, also called a mixer. The mixer multiplies the input reference signal with the signal at the output of the instrumentation amplifier, which is of the same frequency as the reference signal. The product of two sinewave signals with identical frequencies is the sum of two components: 1. a scaled applied force signal and 2. a sinewave signal at twice the original frequency. This sinewave signal at twice the original frequency is removed using a lowpass filter. Reference signal frequency is commonly high compared to the frequency of physiological signals and is in the order of kHz or tens of kHz. Demodulation-based architecture is one of the most popular techniques for measuring capacitance due to its high accuracy. Synchronous demodulators enable accurate measurement of small AC signals in the presence of noise that is several orders of magnitude greater than the signal's amplitude. An example of a synchronous demodulator circuit used for sensor interfaces is the ADA2200 chip by Analog Devices.

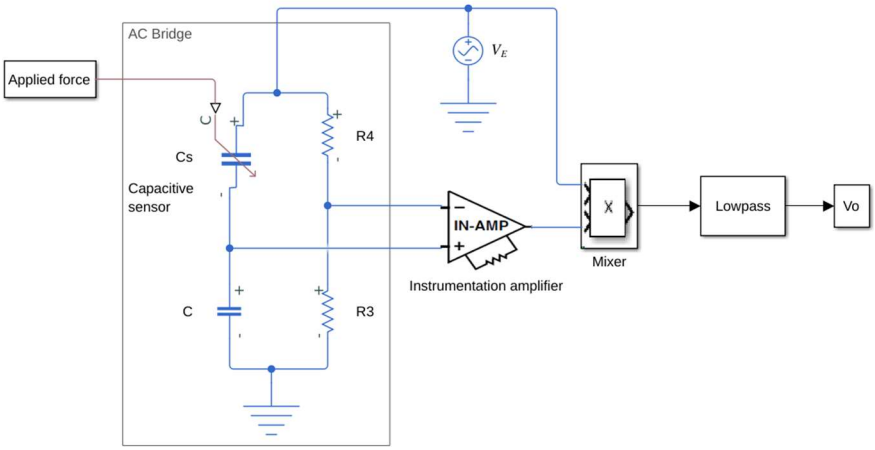


Fig. 4.10 Synchronous demodulation circuit for interfacing capacitive sensor

4.3.6.3 Charge amplifier

A charge amplifier is a charge-to-voltage converter. It is mainly used to connect piezoelectric transducers, including a number of sensors based on piezoelectric transducers such as microphones, accelerometers, ultrasonic receivers, dynamic pressure sensors and so on.

The charge amplifier is shown in Fig. 4.11. It includes the operational amplifiers with the capacitor C_f and resistor R_f in the feedback loop. The capacitance C_f is inversely proportional to the amplitude of the output voltage. The resistor R_f is selected to prevent the amplifier from drifting into saturation. The value of R_f and C_f set the low cutoff frequency of the amplifier: $f_L = 1/(2\pi R_f C_f)$. This charge amplifier acts as an active lowpass filter. Resistor R_i provides electrostatic protection.

The input pin is normally connected to a piezoelectric sensor with an equivalent capacitance C_p shown in Fig. 4.12. Resistor R_i and capacitor C_p provides an upper cut-off frequency $f_H = 1/(2\pi R_i C_p)$. Since we are using single-rail operational amplifier, the positive input of the operational amplifier is connected to $V_{CC}/2$. Therefore, the output voltage $V_o = V_{CC}/2$ with no input.

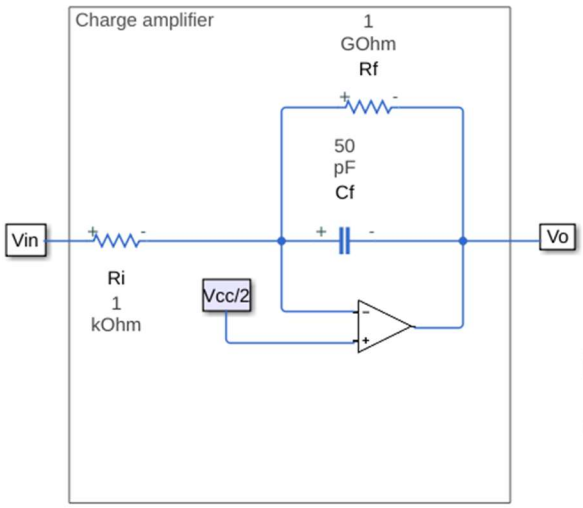


Fig. 4.11 Charge amplifier with a single rail operational amplifier

The circuit that includes a piezoelectric transducer, charge amplifier and additional amplifier at the output is shown in Fig. 4.12 [AD17]. The piezoelectric transducer is modeled as a current source $i_{IN} = dq/dt$ with the capacitance C_p in parallel. Both amplifiers in the circuit are single rail amplifiers, and their voltage range is between 0 V and $V_{CC} = 3.3\ V$. Therefore, $V_{CC}/2$ is used as an offset for both operational amplifiers. The output V_{O1} of the charge amplifier can be calculated as:

$$V_{O1} = \frac{V_{CC}}{2} - V_{Cf} = \frac{V_{CC}}{2} - \frac{q}{C_f} \tag{4.5}$$

Therefore the change in the voltage dV_{O1} is proportional to the change in the charge of the piezoelectric sensor dq/C_f.The output voltage of the circuit is amplified using the non-inverting amplifier and it can be calculated as:

$$V_O = \frac{V_{CC}}{2} - \left(1 + \frac{R_7}{R_8}\right)\frac{q}{C_f} \tag{4.6}$$

Example 4.2: Assume that we connect a piezoelectric quartz-based accelerometer to the charge amplifier [AD17] shown in Fig. 4.12. The parameters of the accelerometer are:

- Range: ±5 g
- Sensitivity: $S_a = 1\ pC/g$. The sensitivity is defined as the change of the charge over the change of acceleration $S_a = \Delta q/\Delta a$.
- Capacitance: $C_p = 90\ pF$

a) Select the values of the components in the circuit and determine low and high cut-off frequencies. Let us assume that the output of the charge amplifier can have a voltage swing of $\pm 0.1\ V$ meaning that it can change by $0.1\ V$ around the reference value.

b) Assume that the signal at the piezoelectric transducer is a sinewave at 20 Hz simulating charge in the range between ±5 pC. Simulate the circuit and show signals V_{Cf}, V_{o1} and V_o.

Solution:

a) The voltage developed across C_f due to a charge Δq is $V_{Cf} = \Delta q/C_f$. By multiplying and dividing the right side of the expression for V_{Cf} with Δa, we get:

$$V_{cf} = \frac{\Delta a}{C_f}\frac{\Delta q}{\Delta a} = \frac{\Delta a \cdot S_a}{C_f}$$

For the voltage swing of $\pm 0.1\ V$ at the output of the charge amplifier V_{o1}, we have the same voltage swing at V_{Cf} (see Equation (4.5)). Therefore, we can compute C_f as $C_f = S_a \Delta a / V_{Cf} = (1\ pC/g \times\ 5\ g)/0.1\ V\ = 50\ pF$. Let us choose R_f to be 1 $G\Omega$.

We can compute the lower and upper cut-off frequencies of the circuit as:

$$f_L = \frac{1}{2\pi R_f C_f} = 3.18\ Hz$$

If we select $R_i = 1\ k\Omega$ then

$$f_H = \frac{1}{2\pi R_i C_p} = 1.77\ MHz$$

In order to observe changes in the output V_o in the range from 0V to 3.3V, we need to amplify the signal V_{o1} 16.5 times ((3.3V/2)/0.1V). Therefore, based on this computation and also based on (4.6), selected values for the resistors are $R_7 = 150\ k\Omega$ and $R_8 = 10\ k\Omega$.

b) Since the sensitivity of the accelerometer is 1 pC/g, a charge change of ±5 pC corresponds to a change in acceleration of ±5 g. In the model, the sinewave signal is differentiated to obtain $i = dq/dt$ and used as an input of the current-controlled source I_{IN} as shown in Fig. 4.12. As can be seen in Fig. 4.13a), the amplitude of the signal V_{Cf} over the capacitor C_f is exactly 0.1 V. The signals are shown in the following time interval [1 s, 1.5 s]. It can also be seen in Fig. 4.13b) that signal at the output of the charge amplifier V_{o1} is amplified around 16 times so that the amplitude of the signal at the output V_o spans almost the whole range between 0 and 3.3V.

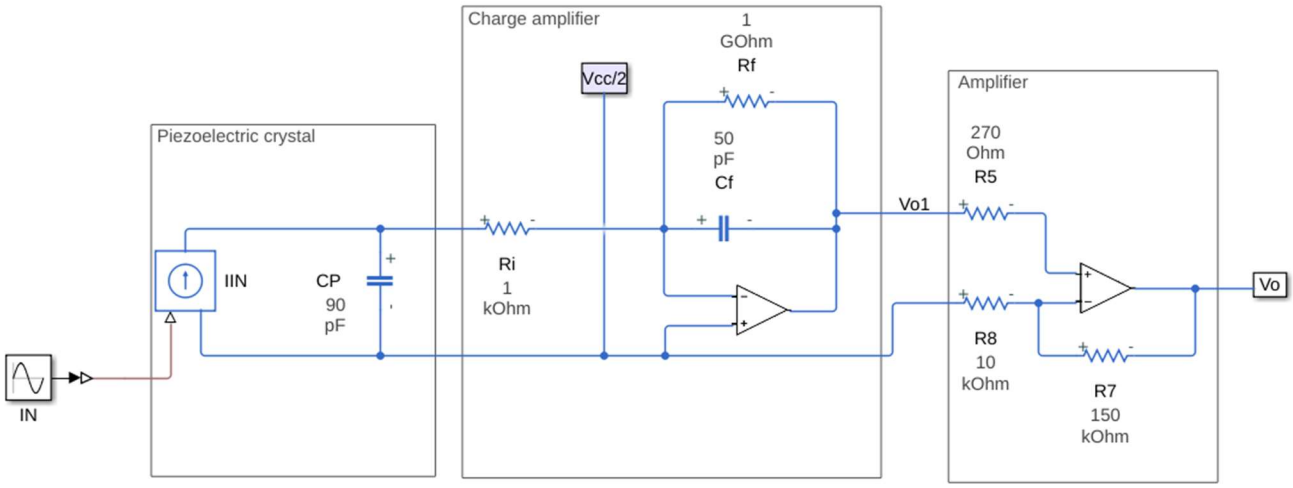


Fig. 4.12 A circuit that includes a model of a piezoelectric sensor, a charge amplifier and a non-inverting amplifier.

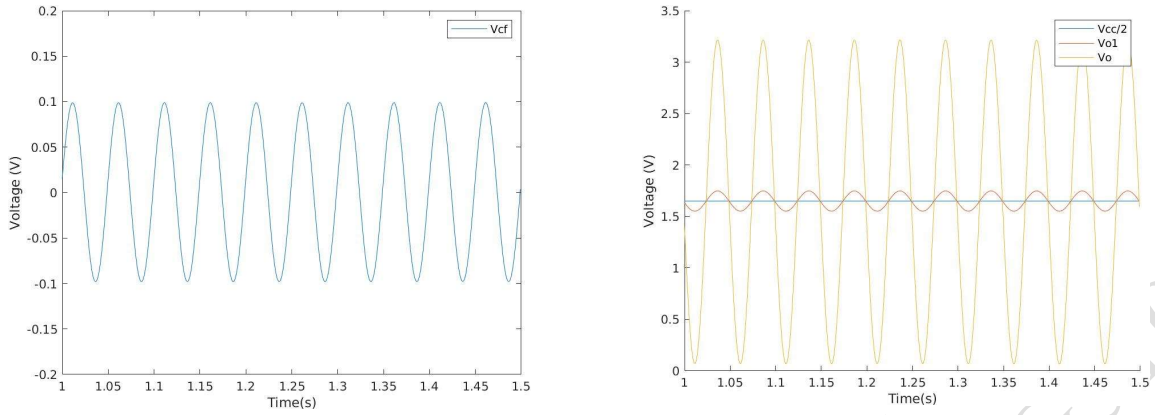


Fig. 4.13 Signals in the circuit shown in Fig. 4.12 in the interval between 1 s and 1.5 s for 20 Hz input sinewave signal, including a) signal V_{Cf} and b) signals V_{o1} and V_o.

4.3.6.4 Transimpedance amplifier

A transimpedance amplifier amplifies a photodiode's reverse-biased current and generates a voltage at the output. It is used in many applications outside of the biomedical area, including compact disc players, infrared remote controls, ambient light sensors, and laser range finding. In the biomedical area, they are used in plethysmography and all imaging applications based on photodetectors. The transimpedance amplifier is shown in Fig. 4.14a). Conceptually, it looks similar to the charge amplifier. The voltage V_o at the output is proportional to the resistance R_f and the photodetector current i_p. Therefore, $V_o = R_f \cdot i_p$. The capacitor C_f determines the highest frequency of interest and prevents the oscillation of the transimpedance amplifier at high frequencies. The oscillations occur since the photodetector can be modeled as a current source, shunt resistor and capacitor connected in parallel. These shunt resistance and capacitance are the reason for potential oscillations at high frequencies.

In Fig. 4.14a), the photodetector current is simulated as $i_p = -1 - \sin(2\pi t \cdot 20Hz)\,\mu A$. Therefore, the expected peak-to-peak voltage at the output is 0.4 V, as shown in Fig. 4.14b). The offset voltage is chosen to be 0.2 V so that it can handle the dark current of the photodiode while still using the bulk of the output voltage range. The cuff-off frequency of the transimpedance amplifier is $f_c = 1/(2\pi R_f C_f) = 295$ Hz.

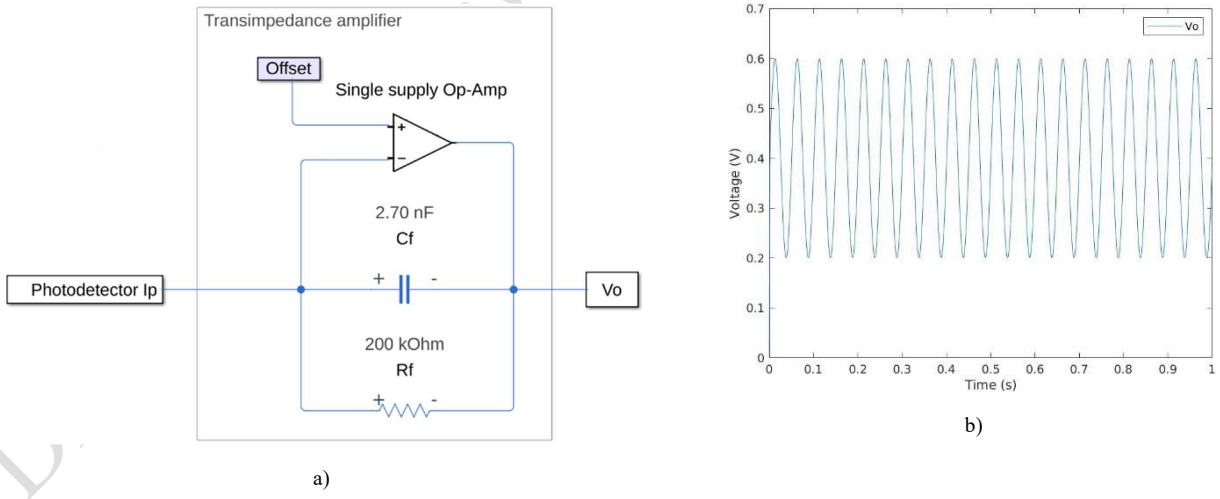


Fig. 4.14 a) Transimpedance amplifier, b) The signal at the output V_o for the input current $i_p = -1 - \sin(2\pi t \cdot 20Hz)\,\mu A$

An example of a commercial transimpedance amplifier is OPA857 by Texas Instruments. The circuit has two transimpedance gains that can be selected by choosing one of two available resistor-capacitor (R_f, C_f) pairs. The amplifier uses a single supply voltage and has a very large bandwidth.

The output of the transimpedance amplifier is often connected to the input of the programmable gain amplifier that will be introduced next. In this case, the programmable amplifier can boost the signal in low light conditions.

4.3.6.5 Programmable gain amplifier

Programmable gain amplifiers (PGA) commonly have a set of gains values that can be digitally programmed or set by a microcontroller or a microprocessor. PGAs are used in biomedical instrumentation in general, as a photodiode amplifier circuit, as an ultrasound preamplifier, and so on.

The amplifiers commonly come with 4 or 8 different values for the gain. The gains are normally multiples of 2, 5 or 10. These gains can be set directly using 2 or 3 additional pins on the PGA chip. Alternatively, they can be programmed using a serial bus such as the Serial Peripheral Interface (SPI) bus [SPI21]. SPI is a serial bus used in embedded systems in which a microprocessor communicates in a full-duplex mode with SPI-supported peripheral devices. Multiple peripheral devices are normally supported through selection with individual chip select (CS) lines.

Programmable gain amplifiers are very important in applications where the signal level can vary significantly and cause the signal at the output of the amplifier to be either too small or saturated. They are often used as a signal conditioning circuit before A/D converter to ensure that the full range at the input of the A/D converter is utilized. An example of a PGA with gains 1 or 2 is shown in Fig. 4.15. The PGA has only one control input that can be set to either 0 V or 5 V. When it is set to 0 V, the switch is up, as shown in Fig. 4.15, and the gain is 1. When the control input is set to 5V, the amplifier acts as a non-inverting amplifier, and the gain is $1 + R_3/R_1 = 2$. This setup of the PGA is used in order to remove the effect of the finite resistance of the switch when the switch is closed [AD08].

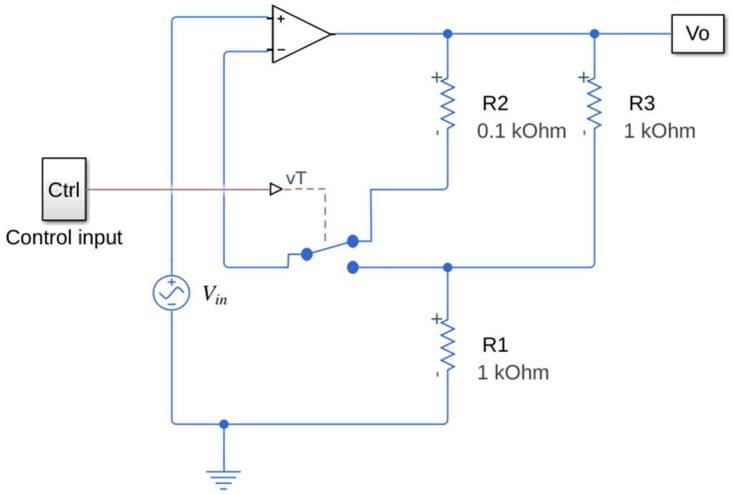


Fig. 4.15 PGA with two selectable gains

Of course, the bandwidth and the gain are inversely related, as mentioned before. Therefore, increasing the gain will decrease the bandwidth of the amplifier. An example of gain and bandwidth for the Burr-Brown PGA103 amplifier is shown in Table 4.3.

Table 4.3 Gain and bandwidth of a commercial PGA: Burr-Brown PGA103

Gain	Bandwidth
1	1.5 MHz
10	750 kHz
100	250 kHz

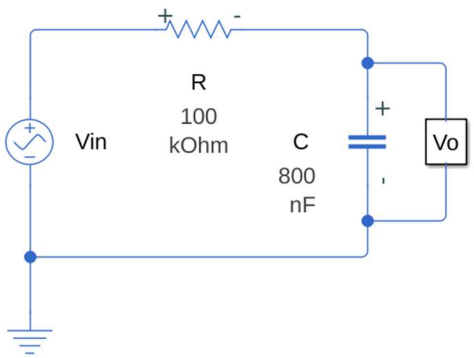
Besides programmable amplifiers, programmable instrumentation amplifiers also exist. An example is the AD8250 instrumentation amplifier from Analog Devices that has two additional control pins for gain control and allows for setting the gain to 1, 2, 5 or 10.

4.4. Analog filters

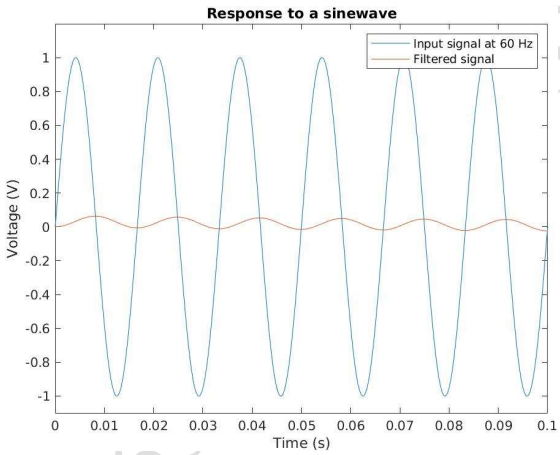
In this section, we will briefly introduce analog filters. Filters that also amplify the signals are called **active filters**. Some of the active filters have already been mentioned before. For example, a differentiator corresponds to the first-order active highpass filter. We start this section with a simple RC filter followed by the second order active lowpass filter. More details about filters can be found in [Wanhammar09].

4.4.1 Passive filter

A simple RC lowpass filter is shown in Fig. 4.16a). Let us define the impedance $Z_c = 1/jC\omega$ as well as **the time constant** $\tau = RC$. The time constant is important since it determines the cutoff frequency of the filter as well as the rise time as a response to a step function. The **cutoff frequency** f_c of the lowpass filter is the frequency selected in a way that all the frequency components of the signal lower than f_c are passed through the circuit unchanged or amplified while the frequency components of the signal higher than f_c are attenuated. The definition related to the magnitude response of the filter will be given later. The cutoff frequency of the filter shown in Fig. 4.16a) is about 2 Hz. The input of the circuit in Fig. 4.16a) is the sinewave signal of the amplitude 1 V and frequency 60 Hz. This signal is attenuated about 16 times and shifted in phase by $\pi/2$ at the output as shown in Fig. 4.16b).



a)



b)

Fig. 4.16 a) The first-order lowpass filter. b) Input signal at 60 Hz (blue line) and filtered signal at the output (red line).

The filter's response to the step function is shown in Fig. 4.17. The step function has a value of 0 V until the instant of 0.2 s, and then its value is 5 V. The capacitor is charged fully after about five time constants. After one time constant, the voltage across the capacitor is about $0.63 \cdot V_{in}$.

Now, let us compute the magnitude and phase response of the RC filter. The transfer function in the frequency domain can be written as:

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{\frac{1}{j\omega c}}{R + \frac{1}{j\omega C}} = \frac{1}{1 + j\omega RC}$$

where $\omega = 2\pi f$ is the angular frequency. The amplitude and phase responses are then:

$$A(j\omega) = \frac{1}{\sqrt{1 + (2\pi f)^2 (RC)^2}} = \frac{1}{\sqrt{1 + (2\pi f\tau)^2}}$$

$$\phi(j\omega) = \text{atan}(-2\pi f\tau)$$

From the amplitude response, we can determine the frequency where the amplitude drops by half (by 3 dB). This frequency is the **cutoff frequency**, and it can be shown that it is:

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau}$$

For this filter, we used capacitor $C = 800\ nF$ and resistor $R = 100\ k\Omega$. Then the cut-off frequency is $f_c = 2\ Hz$.

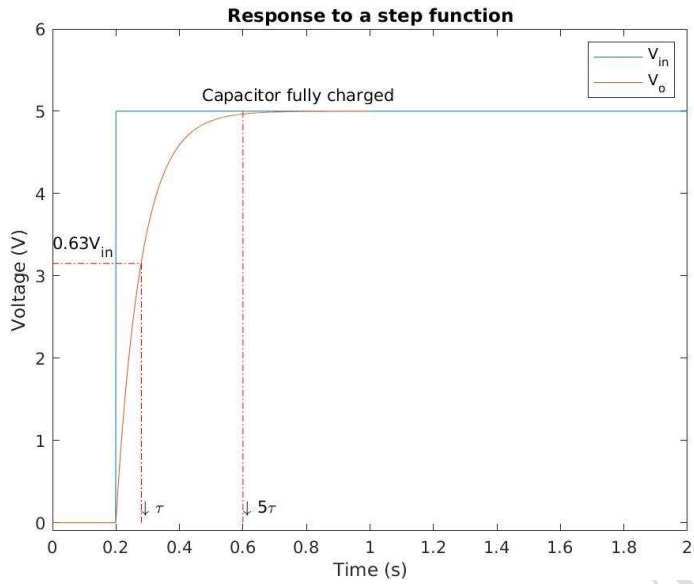


Fig. 4.17 Response to a step function. The input voltage is 0 V until 0.2 s; after that, it remains at 5 V.

4.4.2 Active filter

Active filters are used frequently because they amplify while also performing filtering. They can be implemented in different configurations. One of the most popular architectures is the Sallen-Key second order lowpass active filter shown in Fig. 4.18. This is a second-order filter with an attenuation of 40 dB per decade. This filter is widely used because it can be implemented to have characteristics of the most popular filter types, such as Butterworth or Chebyshev [Webb18]. The filters are also easily cascaded to create higher order filters. They can be implemented as well as highpass or bandpass by exchanging places of resistors and capacitors.

The cutoff frequency of the filter is determined by:

$$f_c = 1/2\pi\sqrt{R_1 R_2 C_1 C_2}$$

In order to design the filter, we use the following approximate formula for determining the cutoff frequency based on the required attenuation A_v at the frequency of interest. Let us assume that we would like to attenuate f=60 Hz frequency 10 times ($A_v = 0.1$).

$$f_c = f/\sqrt[4]{(1 - A_v^2)/A_v^2}$$

After plugging the numbers for the frequency of interest and attenuation, we obtain that $f_c = 20\,Hz$. Then, let us assume that $C_2 = 2 \cdot C_1 = 200\,nF$. Also, if we assume that $R_1 = R_2 = R$, we obtain from $f_c = 1/(2\pi\sqrt{2}RC_1)$ that the resistance is R=59 kΩ. We can choose a standard resistor value instead, for example, R=69 kΩ.

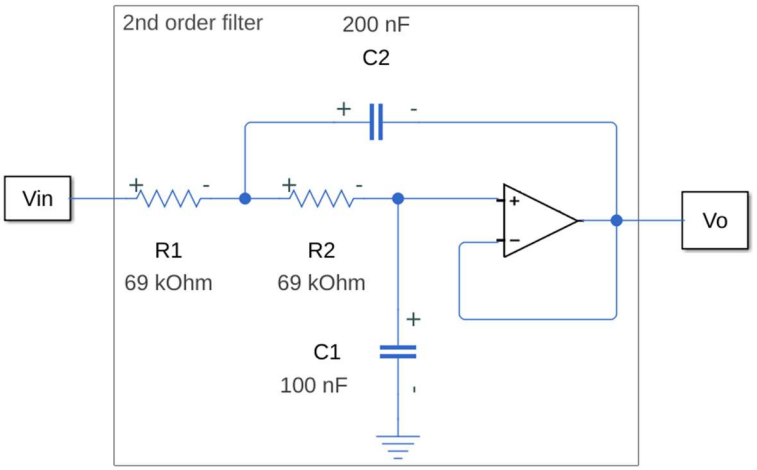


Fig. 4.18 Sallen-Key second order lowpass active filter

Its Bode diagram is shown in Fig. 4.19. For the selected resistors and capacitors, the cutoff frequency is 16.2 Hz and the attenuation at 60 Hz is 0.074 or -22.7 dB which is smaller than the required attenuation of 0.1.

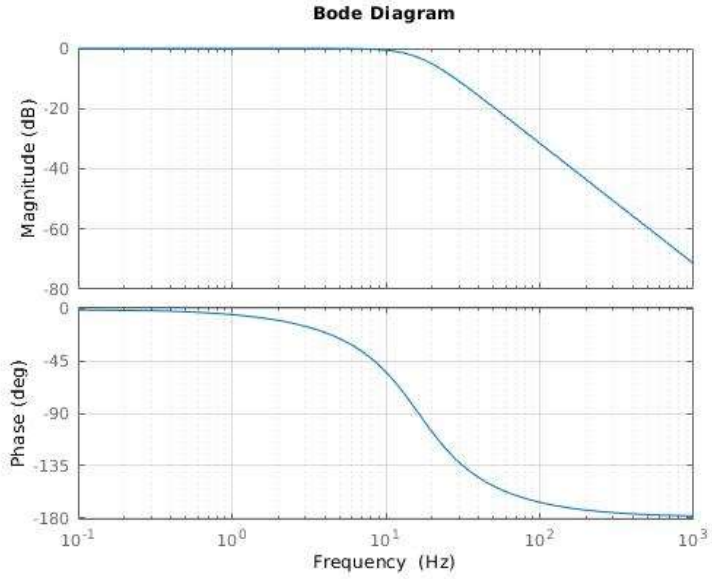


Fig. 4.19 Bode plot of the amplitude and phase of the Sallen-Key filter

Please note that this section does not introduce bandpass and highpass filters. However, they can be made by modifying the Sallen–Key topology [Wanhammar09].

4.5. Analog to digital converter

4.5.1 Sampling

4.5.1.1 Sampling theorem

An analog signal is defined at every point t of the signal $x(t)$. Discrete signals, on the other hand, are defined only at the sampling points $x(nT_s)$, where n is the sampling number. Here, the signal $x(t)$ is sampled every T_s seconds, where T_s is called the **sampling period** and $f_s = 1/T_s$ is the **sampling frequency**.

To accurately reproduce the analog input data from its samples, the sampling rate f_s must be at least twice as high as the highest frequency expected in the input signal. This is known as a sampling theorem [Oppenheim98]. Half of the sampling frequency is known as the **Nyquist frequency** f_h.

$$f_s = 2 \cdot f_h$$

The discrete signal is commonly presented in a way that time t in the continuous signal is replaced with nT_s in the discrete signal representation. For example, let us consider a breathing signal at 15 breaths per minute (0.25 Hz) modeled as a sinusoid with a sinusoidal interferer at 60 Hz:

$$x(t) = 1.5 + \sin(2\pi \cdot 0.25t) + 0.25 * \sin(2\pi \cdot 60t) \tag{4.7}$$

After sampling, the discrete signal $x(nT_s) = x(n)$ is:

$$x(n) = 1.5 + \sin(2\pi \cdot 0.25nT_s) + 0.25 * \sin(2\pi \cdot 60nT_s) \tag{4.8}$$

4.5.1.2 Antialiasing

Sampling analog signal below $2f_h$ generates **aliased components** at the frequencies determined by: $f_{alias} = |f_l - kf_s|$ where f_l is the frequency component of the sampled signal with a higher frequency than the Nyquist frequency, and k is the harmonic number $k = 0, \pm1, \pm2, \ldots$. We are interested only in the aliased components in the range between $-f_s/2$ and $f_s/2$.

Example 4.3: 10 Hz sinewave signal is sampled at 12 Hz.

a) Show the signal at the output of the A/D converter.

b) What is the fundamental frequency of the signal at the output?

Solution: The signals are shown in Fig. 4.20. The blue line represents a 10 Hz sine wave signal. After sampling, the fundamental frequency is $f_{alias} = |f_l - kf_s|$ which is 2 Hz for k=1. Samples at the sampling period of 1/12 s are shown using red dots. The red line is the interpolated signal that has a frequency of 2 Hz.

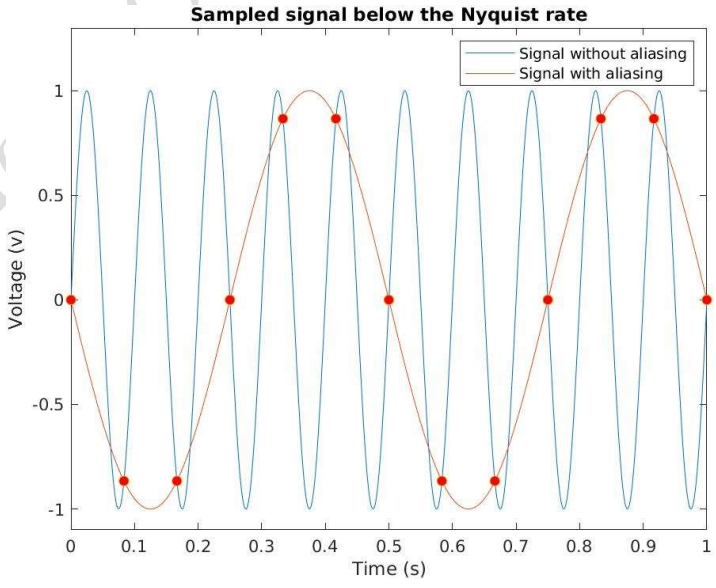


Fig. 4.20 Blue line shows a 10 Hz sinewave signal while the red line with red dots shows samples from the 10 Hz sine wave sampled at 12 Hz. The red line is a sinewave that is interpolated between the red samples.

Example 4.4: The signal shown in (4.7) is sampled at $f_s = 80\ Hz$.

a) Determine if aliasing occurred.

b) Simulate and draw the signal after sampling.

Solution:

a) The sampled signal will then be:

$$x(n) = \sin(2\pi n \cdot 0.25/80) + 0.25 * \sin(2\pi n \cdot 60/80) = \sin(2\pi n \cdot 0.25/80) - 0.25 * \sin(2\pi n \cdot 20/80)$$

As can be seen, $sin\ (2\pi n \cdot 60/80) = -sin\ (2\pi n \cdot 20/80) = -sin\ (2\pi n/4)$. So, the frequency component from 60 Hz aliased to -20 Hz. The same result can be obtained using $f_{alias} = |f_l - kf_s|$=20 Hz for $f_l = 60Hz$ and $k = 1$.

b) The aliased signal is shown in Fig. 4.22a) as a blue signal at the frequency of 0.25 Hz modulated with the frequency of 20 Hz.

Frequency components above the highest frequency of interest need to be removed. However, in practice, they cannot be removed but only attenuated, which is done using a lowpass filter called an **antialiasing filter**. Fig. 4.21 shows an antialiasing filter followed by an A/D converter ADC2. The filter has already been introduced in Fig. 4.18. In addition, we show the effect of sampling without using an antialiasing filter. This is done by directly connecting the A/D converter ADC1 to an input signal. We know that the filter presented in Fig. 4.18 attenuates the signal at 60 Hz by about ten times (20 dB). Therefore, as shown in Fig. 4.22b), there is still aliasing even if the antialiasing filter is used; however, the aliased frequency component is attenuated by 22.7 dB as explained in Section 4.4.2. In the time domain (Fig. 4.22a), the red line shows the sampling signal after aliasing. The 60 Hz interference signal is attenuated significantly, but it is not removed – it appears as a 20 Hz signal.

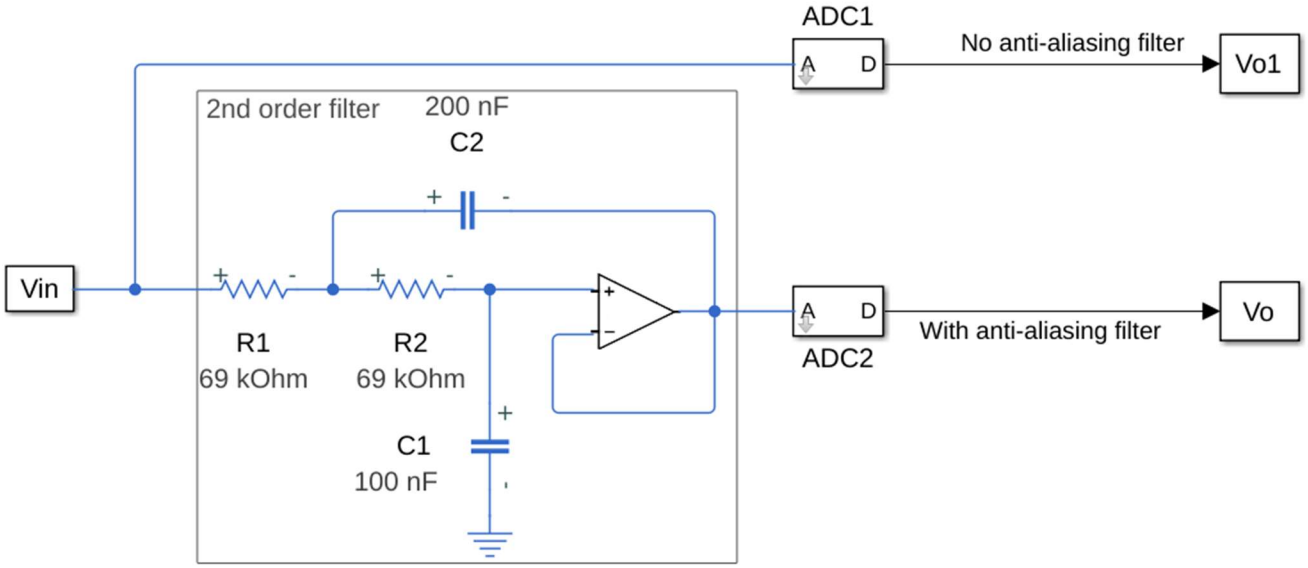
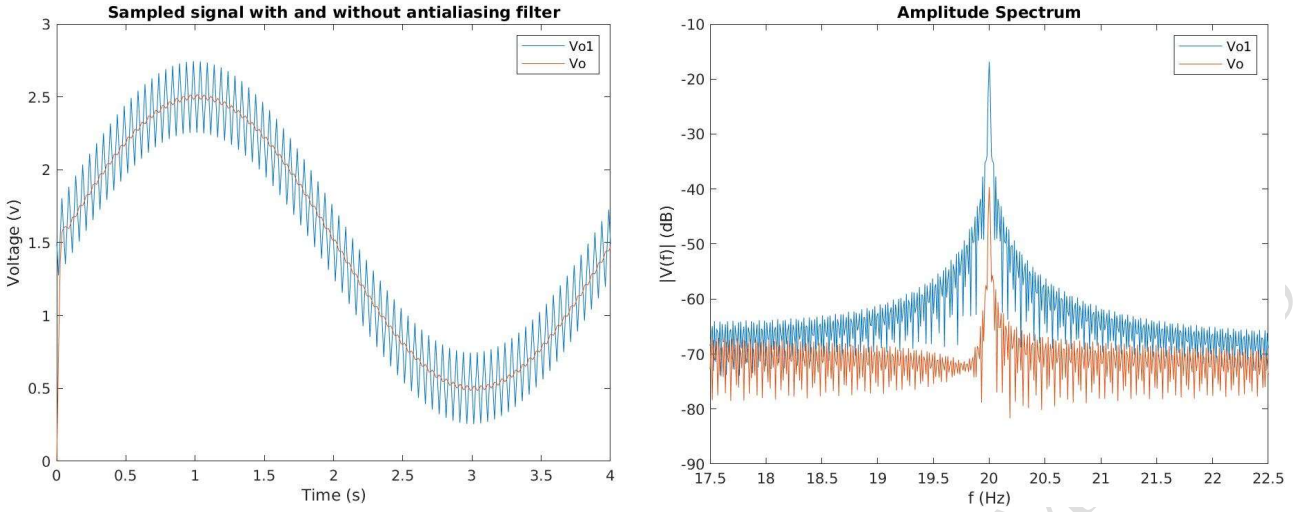


Fig. 4.21 A circuit with two A/D convertors for analyzing the effects of aliasing with and without an antialiasing filter.



a) b)

Fig. 4.22 Signal sampled at $f_s = 80\ Hz$ without (blue line) and with (red line) the antialiasing filter. a) Time-domain signal. b) Power spectrum. There is a frequency component at 20 Hz, which results from the aliasing of the 60 Hz sinewave signal. The magnitude of the frequency component at 20 Hz is reduced by 22.7 dB using the antialiasing filter.

4.5.1.3 Quantization

Quantization is the conversion of a discretized analog signal into an integer number. The number can be positive or negative, or only positive depending on the range of the A/D converter. The transfer function of the A/D convertor is a staircase-like function with the input analog signal on the abscissa and the digital signal on the ordinate. The digital signal is presented using integers, often in a binary format. An example of the transfer function of an ideal 3-bit A/D converter is shown in Fig. 4.23. Here, the abscissa represents normalized input voltage where V_{FS} is the full-scale voltage of the A/D converter and V_{in} is the input signal at the A/D converter. In Fig. 4.23, the ordinate represents the binary value at the output of the ADC.

The minimum change in voltage required to change the output code level is called the **least significant bit voltage** V_{LSB}. The **voltage resolution** of the A/D converter is equal to V_{LSB} and it is computed as: $V_{LSB} = V_{FS}/2^N$, where N is the number of bits of the A/D converter. In Fig. 4.23, relative V_{LSB} corresponds to the change of $0.125 \cdot V_{FS}$. Also, the line of infinite resolution is shown as well – in the case of an A/D converter with a very large number of bits V_{LSB} would tend towards zero.

After quantization, the signal can be reconstructed as follows:

$$V_o = V_{FS} \sum_{i=0}^{N-1} b_i 2^{-(N-i)} \tag{4.9}$$

Here b_0 corresponds to the least significant bit (LSB) of the digital signal and $b_{N-1}b_{N-2} \ldots b_1 b_0$ represents the N-bit binary number at the output of the A/D converter.

Quantization error represents the difference between the input value and the value that is reconstructed at the output: $e_c = V_O - V_{in}$. Quantization error is zero only in the points $V_{LSB} \cdot n$, where $n = 0, \ldots, 2^N - 1$. We will assume that the quantization error is equally likely in the interval $[-V_{LSB}/2, V_{LSB}/2]$ and therefore, it follows a uniform distribution. This will be important for uncertainty quantification in the following chapters.

Example 4.5: A/D convertor operates between 0 V and 5 V, and its transfer function is shown in Fig. 4.23.

a) What is the output of the A/D converter if the input is $V_{in} = 2.25\ V$
b) What is the recovered output in volts?
c) What is the quantization error?

Solution:

a) Full-scale voltage is $V_{FS} = 5V$. The relative voltage at the input is $2.25\ V/5\ V = 0.45$. The binary output for the A/D converter is $b_2 b_1 b_0 = 100$.
b) The recovered output $V_O = 5V \cdot (b_2 2^{-1} + b_1 2^{-2} + b_0 2^{-3}) = 5V \cdot 2^{-1} = 2.5V$
c) Therefore, the quantization error is $e_c = V_O - V_{in} = 0.25V$

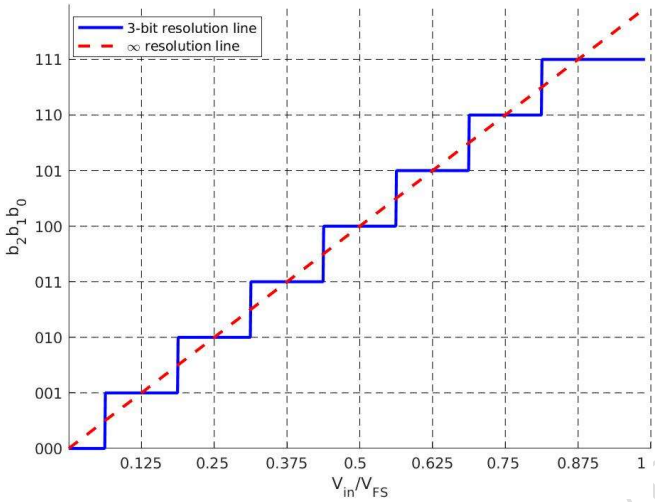


Fig. 4.23 Transfer function of a 3-bit A/D converter

4.5.1.4 A/D conversion steps

A model of the A/D converter is shown in Fig. 4.24. The main blocks are the limiter, sample and hold circuit and the quantizer. If the signal at the input is smaller than zero or larger than the maximum voltage applied to the A/D converter, the output of the limiter will be saturated to zero or maximum voltage, respectively. Of course, the minimum voltage does not need to be zero and can also be negative. The **sample and hold** circuit converts the analog signal into the discrete signal that keeps the same value for the duration of the sampling period. This value is then quantized and converted into a digital signal. Finally, the **quantizer** performs the following operation:

$$V_o = round(V_{in}/V_{LSB})$$

The difference between the discrete and the digital signal is that the discrete signal can take any value in the range of the A/D converter that the analog signal can take, while the digital signal can take only 2^N values where N is the **bit resolution** of the A/D converter. In this A/D converter, the output is zero between 0 and $V_{LSB}/2$, binary one between $V_{LSB}/2$ and $3V_{LSB}/2$, and so on.

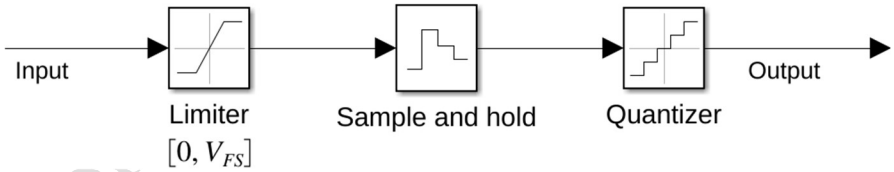


Fig. 4.24 Functional block diagram of an A/D converter

Fig. 4.25 shows the results of the simulation of the A/D converter shown in Fig. 4.24 with the following characteristics: sampling rate $f_s = 12\ Hz$, number of bits N=4, minimum voltage level 0 V, maximum voltage level 5 V. The input signal shown using the blue line is a 0.25 Hz sine wave signal whose amplitude is in the range [0.5 V, 2.5 V]. The signal at the output of the sample and hold block is shown as a red line. The dots on the red line are the voltage values sampled at the specific time instant. After the signal is sampled, its value is kept constant for the duration of the sampling period. The quantizer converts the value of the discrete sample after the sample and hold block into one out of 2^N integers. These values are normally given in binary form. However, here we modeled the output of the A/D converter as the reconstructed signal shown in (4.9). Of course, with increasing the resolution of A/D converter to, for example, N=8 bits, the quantization error would become smaller, and it would be difficult to observe the difference between the output of the sample and hold circuit and the reconstructed output of the quantizer.

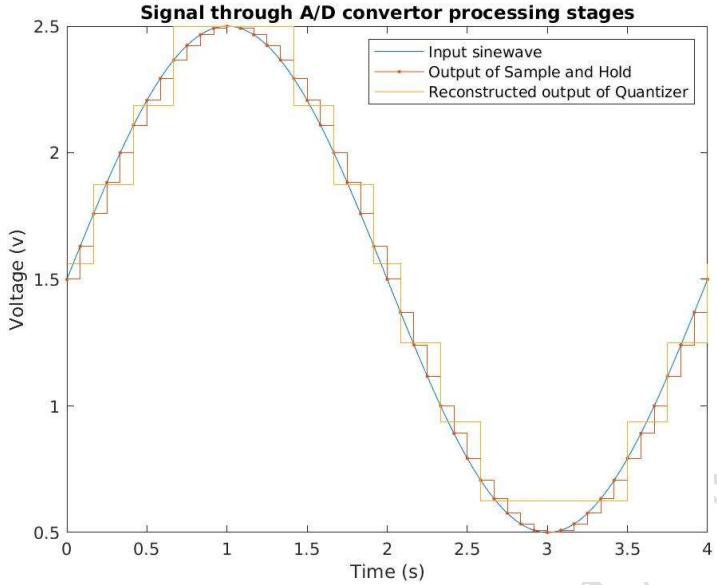


Fig. 4.25 Blue line represents a sinewave signal at the input of the 4-bit A/D converter, the red line is the signal obtained after the sample and hold block, while the yellow line is the scaled signal obtained at the output of the quantizer. Scaling is done by dividing the signal with V_{FS}.

4.5.2 Errors during A/D conversion

Quantization error has already been introduced. This error contributes to the distortion of the signal at the output of the A/D converter. In order to understand this section, we will introduce several terms related to **periodic waveforms**. The **fundamental frequency** is the lowest frequency of a periodic waveform. Multiples of the fundamental frequency are called **harmonics**.

Signal to noise ratio (SNR) of an A/D converter is the measured ratio of the power of the signal and the noise at the output of the A/D converter, where the noise can come from different sources and can include the quantization noise:

$$SNR_{DB} = 10log_{10}(P_{signal}/P_{noise}) \tag{4.10}$$

The theoretical signal-to-noise ratio for an ideal N-bit converter with a sine wave input is given by

$$SNR = (6.02N + 1.76)\, dB \tag{4.11}$$

where N is the bit resolution of the A/D converter.

Let us consider a sine signal at the frequency of 1.1 Hz centered between 0 V and 1 V corresponding to a pulse waveform sampled at 80 Hz. We compute SNR based on the definition (4.10) while changing the resolution of the A/D converter from 4 to 16 bits (Fig. 4.26). Computed SNR matches well the approximation shown in (4.11).

Signal-to-Noise-and-Distortion Ratio (SINAD) is the measured ratio of the power of the signal to the power of noise and distortion at the output of the A/D converter. Here, the signal is normally the sine wave at the fundamental frequency. The noise and distortion include the power of all nonfundamental components of the signals up to the frequency $f_s/2$ excluding the DC value. Harmonics of the original signal are also considered distortion. Please note that different definitions of SINAD exist in other fields, such as communication.

The effective number of noise-free bits in an A/D converter is normally smaller than the resolution of A/D converter. Therefore, the **effective number of bits** is defined as ENOB=(SINAD-1.76)/6.02. Normally, the last two bits at the output of the A/D convertor vary when the input signal is constant, and we can effectively use only N-2 bits of the A/D converter.

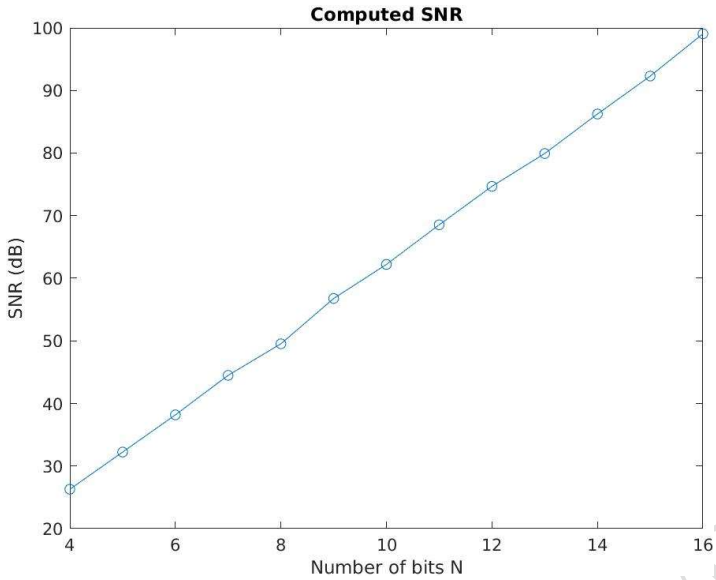


Fig. 4.26 Computed SNR for the A/D converters based on (4.10) when the number of bits changes between 4 and 16 for the signal $V_{in}(t) = 0.5V + 0.5V \cdot sin(2\pi f_i\, t)$.

Example 4.6:. Let us consider a 16-bit A/D converter and the following signal: $V_{in}(n) = 0.5\text{V} + 0.5\text{V} \cdot \sin(2\pi f_i T_s n) + v \cdot randn(0,1)$. Here we add to the signal random Gaussian noise whose standard deviation is v. Compute SNR, SINAD and ENOB when:

a) v=0,
b) v=V_{LSB},
c) v=$2V_{LSB}$.

Solution:

Matlab code is provided for computing these values on the book website. The results are summarized in Table 4.4. The results shown in the table are expected for the following reasons. SINOD and SNR have almost the same values since there are no additional harmonics. It is known that more than 95% of the normal random variable will be between two standard deviations [-2 v, 2v] in case b). In the case b), [-2 v, 2v] = $\left[-2V_{LSB,}\ 2V_{LSB}\right]$, and therefore, 2 bits (representing 2^2=4 LSB levels) are lost due to noise.

For case c), 95% of the generated noise will be in the range of [-2 v, 2v] = $\left[-4V_{LSB,}4V_{LSB}\right]$. Therefore, the range of $8V_{LSB}$ can be presented using 3 bits ($2^3 = 8$). Therefore, we observe the loss of 3 bits in the effective number of bits.

Table 4.4 Computed SNR, SINAD and ENOB for **Example 4.6** for 16-bit A/D converter.

Feature	SNR (dB)	SINAD (dB)	ENOB (bits)
a)	99	98.8	16.14
b)	87.7	87.6	14.26
c)	81.6	81.5	13.2

4.5.3 A/D converter types

Four main types of A/D converter architectures include flash, pipelined, successive approximation register and sigma-delta A/D converters. The choice of an A/D converter depends on the resolution and sampling rate, as well as the power consumption of the A/D converter. High resolution and high sampling rate cannot be achieved at the same time. The speed of the A/D converters drops, and their resolution increases from flash to sigma-delta A/D converters. Since speed is normally not a concern in biomedical applications, successive approximation register and sigma-delta A/D converters are the most common types. A successive approximation A/D converter converts a continuous analog waveform into a digital representation via a binary search through all possible

quantization levels before finally converging upon a digital output for each conversion. Sigma-delta converters have high resolution, low power consumption and low cost. A significant portion of the conversion is performed digitally. Details about types of A/D converters can be found in many textbooks, including [Webb18], [Pelgrom17]. Instead of presenting them here, we will focus on A/D convertor types that are important in connecting different types of sensors/transducers.

4.5.3.1 Multiplexed versus simultaneous sampling

A/D converters commonly support multiple analog inputs; therefore, they are called **multi-channel A/D converters**. Here, the channel means the input signal. The benefit of multiplexing is fewer numbers of single-channel A/D converter chips required, saving the area on a printed circuit board as well as power and cost. Multi-channel A/D converters normally convert a signal from each input channel sequentially in a time-multiplexing fashion using an input multiplexer. An example of an integrated 3-channel data acquisition system that includes a multiplexer, programmable gain amplifier and an A/D converter in the same chip is shown in Fig. 4.27. Most integrated multiplexed A/D converters provide automated channel switching, custom sequencing between channels, and configurations with different input ranges and error calibration options for each channel [Pachchigar21].

Some common issues in multiplexed A/D converters are related to potential large amplitude changes between channels when switching from one channel to the next. To handle large amplitude changes, the amplifier (or PGA) must have a wide bandwidth and fast settling time. Therefore, dynamic performance is normally reported as output voltage settling time. An example settling time for Analog Devices AD74412R is 90 µs at a 10 V step.

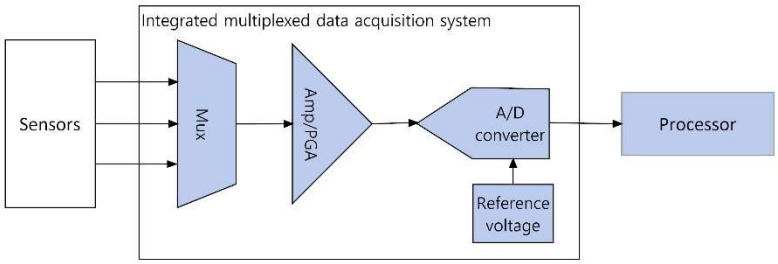


Fig. 4.27 Multiplexed data acquisition system [Pachchigar21]

In multiplexed A/D converters, each sample from a different channel is phase-shifted (delayed) relative to the sample in another channel. Simultaneous sampling means that the signals from different channels are all sampled at the same time. This is useful in applications that measure phase angle between signals, such as motor control or bioimpedance measurements. If it is necessary to sample signals simultaneously, then multiple A/D converters can be used. In the last two decades, main chip manufacturers, such as Analog Devices, Maxim Integrated and others, developed integrated solutions allowing simultaneous sampling. The idea behind simultaneous sampling is based on using multiple parallel sample and hold circuits that sample signals from different channels simultaneously and then holds them until they are processed. Another integrated simultaneous sampling solution contains parallel A/D converters in a chip.

4.5.4 Integrated special-purpose A/D converters

A/D converters can be integrated with sensors, amplifiers, processors, and so on. In this way, they represent smart solutions that provide a digital interface to the rest of the system. We will cover below the following integrated A/D converters:

- Integrated **A/D converters with programmable gain amplifiers**
- **Capacitive to digital converters**
- **Time to digital converters**.

Some other examples of integrating A/D converters with other components include:

- **Audio A/D converters** are high-resolution A/D converters designed to sample several channels from microphones
- **Digital Temperature Sensors**, which include a temperature sensor and complete data acquisition system
- ***Isolated A/D converters*** that allow for galvanic isolation between the analog input and digital output, which is very useful for medical applications
- **Current sensing** A/D converters normally convert voltage on an external resistive load that is added externally to measure the current
- **Current to digital converters** convert the signals of photodiodes or other sensors with current signal output into a digital signal. An example includes a component AS89010, a 16-bit 4-channel A/D converter from AMS that has sensitivity up to 20 fA/LSB and allows for direct connections of four photodiodes.
- **Current to frequency converters** convert a current signal from the photodiode into a square wave with frequency directly proportional to light intensity (irradiance) on the photodiode. If the photodiode is integrated on the chip together with the current to frequency converter, then they are called **light to frequency converters**.

4.5.4.1 A/D converters with PGAs

The magnitude of the input signal of the A/D converter should be fairly close to its full-scale voltage range. However, the output voltage of transducers can have a wide voltage range. In addition, the baseline voltage of the signal might change over time, causing saturation at the output of the amplifier. Therefore, a constant amplifier gain is not satisfactory in situations where the input of A/D converters can have a wide input range. So, programmable gain amplifiers (PGAs) are often integrated to increase the dynamic range of A/D converters, as shown in Fig. 4.27. This configuration allows for controlling the gain of the amplifier through the common A/D converter interface.

To understand the need for different gains, let us consider (4.11). If we are able to "add" one bit resolution to the A/D converter, this will improve its SNR by about 6 dB. If the voltage resolution of the A/D converter is equivalent to $V_{LSB} = 2\ mV$, then the A/D converter cannot resolve signals smaller than 2 mV. However, if there is a built-in PGA that can amplify the input voltage by 2, for example, then the A/D converter will be able to resolve 1 mV signals at the input of the device. Therefore, amplification, in this case, would effectively increase the dynamic resolution of this A/D converter by 6 dB.

A/D converters with PGA allow for direct connection with sensors. In the case of strain gauges, the differential output of the bridge would be connected to the input of the A/D converter with PGAs. Therefore, inputs to the A/D converters with PGA chips are commonly differential.

4.5.4.2 Capacitance to digital

Capacitance to digital converter (CDC) is the component that allows for interfacing directly to a capacitive transducer. Biomedical applications include blood pressure measurements, sweat detection and respiratory rate measurement [Jia12].

There are several architectures of capacitance to digital converters. We will explain an architecture with a sigma-delta modulator followed by a digital filter. The capacitive transducer is connected externally. One plate is connected directly to the excitation signal. Fixed frequency is applied to the capacitor during the conversion. The other plate is connected directly to the input of the converter. Since the capacitor is not connected to the ground, it is a floating capacitive transducer. It is possible to measure the capacitance of a single or differential floating capacitive transducer. The accuracy of the conversion is in the order of fF. The capacitance is measured as $C = Q/V$, where the V represents the excitation voltage, and Q represents the measured charge.

4.5.4.3 Time to digital converters

Time to digital convertors measure the time between the start and stop of an event. They are used wherever time-interval measurement is required, such as time-of-flight measurements, or measurement and instrumentation applications such as digital scopes [Henzler10]. Since a large number of applications in biomedical instrumentation require time measurements, we see a potential for using the time to digital converters in this field.

The traditional approach to time-to-digital conversion is first to convert the time interval into a voltage using an integrator. Then, in a second step, this voltage is digitized by a conventional A/D converter. Another fully digital approach includes a counter that counts between the start and the stop event. The resolution of this time to digital converter depends on the counter's clock frequency – the higher the frequency, the higher the time resolution. In this case, the time resolution is limited to several hundreds of picoseconds since the clock frequency can be at most in the order of several GHz. However, this is more than enough resolution for the biomedical applications discussed in this book.

4.5.4.4 Integrating conditioning circuitry and A/D converters

Several different integrated solutions require only sensors to be added externally – all other conditioning and conversion electronics are in the chip. One example is the bridge transducer A/D converter. This circuit requires only a bridge to be connected externally. It produces a digital signal the output. An example is the component AD7730 by Analog Devices. It consists of a high impedance input buffer connected to a 4-gain PGA followed by a sigma-delta A/D converter and digital lowpass filter. In addition, the component allows for serial communication with a microcontroller for parameter setting and A/D converter outputs as well as offset control, placing the device in a standby mode for power reduction, and so on.

High integration of electronic components significantly reduces the number of components on the medical device's printed circuit board, allowing for designing miniature wearable devices.

4.6. Generating signals

4.6.1 D/A converters

A **digital-to-analog converter** is a device that converts a digital code to an analog signal in the form of a current or voltage. The output of a D/A converter is used to drive various devices, including motors, mechanical servos, bioimpedance monitoring devices, and so on. D/A converters are also commonly used as a component in A/D converters, microcontrollers and digital systems. D/A converters produce discrete output as a response to a digital input word; therefore, their transfer function is the inverted transfer function of A/D converters shown in Fig. 4.23. Let N be the number of bits at the input of the D/A converter. The analog output of the D/A converter is proportional to the ratio of the digital word (code) at the input and the maximum number of discrete output values 2^N.

4.6.1.1 The architecture of a D/A converter

As with A/D converters, we will not present different D/A converter architectures in detail. Several common architectures include voltage divider, segmented, ladder, and sigma-delta. To find out more about D/A architectures, please refer to [Kester05a].

Fig. 4.28a) shows a high-level block diagram of a D/A converter, including an input register, decoder, reference voltage source, D/A architecture itself and an amplifier. These components are commonly integrated on a chip. The input to the D/A is an N-bit word. The simplest D/A converter architecture is a register string network that has 2^N equal resistors and 2^N switches. Therefore, the input N-bit word must be decoded and converted into a 2^N-bit word that contains only one logic one at the position that corresponds to the digital input. The output is determined by closing one out of 2^N switches to point into a particular location on the resistor string, as shown in Fig. 4.28b). When there is a code transition, one switch will be turned off and another turned on; therefore, we say this is a low glitch architecture.The major disadvantage of this architecture is a large number of resistors and the need for the resistors to have the same values. However, the resistor string D/A architecture can be used as a component (or segment) in a more complex D/A architecture. For example, D/A converters with resolutions from 8 to 16 bits are commonly designed as segmented architectures.

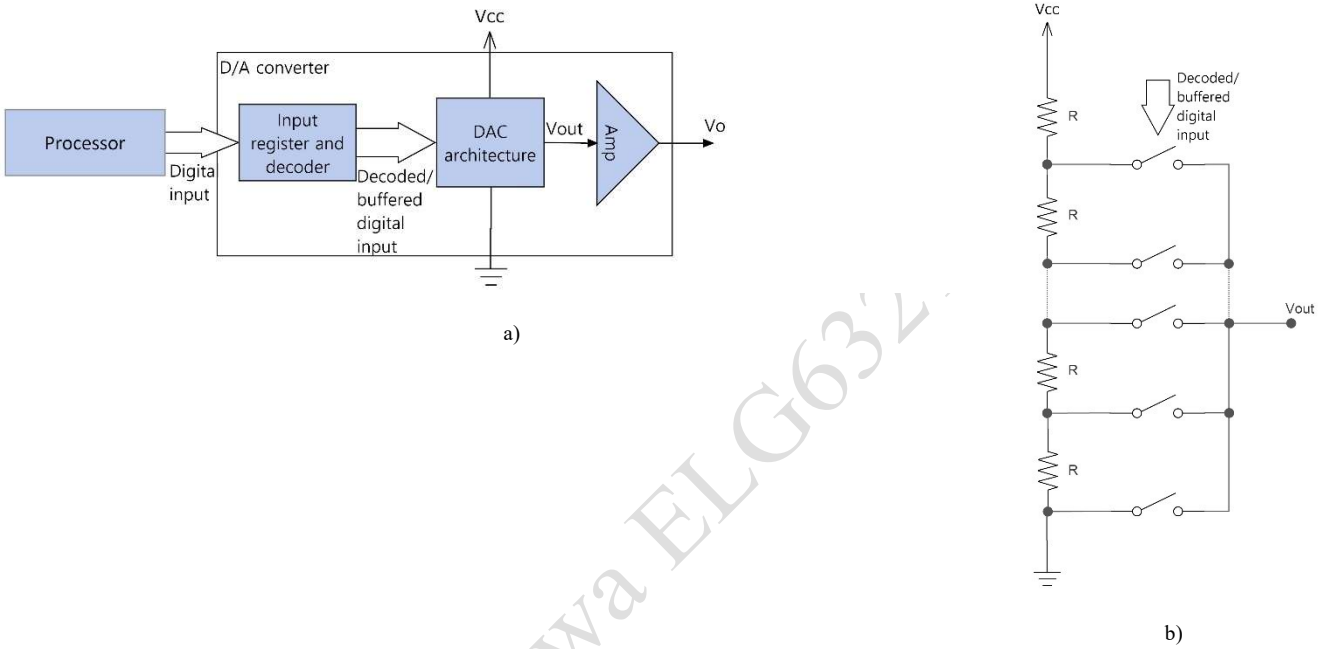


Fig. 4.28 a) A block diagram of a D/A converter, b) Simplified resistor string structure

The output of the D/A converter is determined as:

$$V_{OUT} = A \cdot V_{FS} \cdot W/2^N$$

where W is the decimal equivalent of the binary code word that represents the digital input to a D/A converter, N is the resolution of D/A converter, A is the gain of the output amplifier. V_{FS} is the full-scale reference voltage. In Fig. 4.28a), $V_{FS} = V_{cc}$.

4.6.1.2 Errors during D/A conversion

Specifications related to D/A converters can be grouped into static or DC specifications and time and frequency domain specifications [Mercer21]. Common static specifications include gain error, offset error, differential and integrated nonlinearities. Common time domain specifications are output voltage settling time and digital to analog glitch impulse. Frequency domain specifications include spurious-free dynamic range (SFDR), total harmonic distortion (THD), and signal-to-noise ratio (SNR).

Let us start with static specifications. **Gain error** is the deviation of the slope of the converter's transfer function from that of the ideal transfer function over the full scale, and it is given as a percentage of the full-scale range. In the absence of gain error, the **offset error** is the deviation of the output of the D/A converter from the ideal output, which is constant for all the input codes. It is expressed in mV normally. For example, a 10-bit D/A converter with $5\ V$ reference voltage can have a $1.5\ mV$ offset error. **Integral nonlinearity** (INL) is the deviation of the actual output voltage measured for a certain input code from the ideal output voltage for that code. INL is calculated for all input codes after offset and gain errors are removed. It is normally given as a figure showing INL versus the digital input codes and also as the maximum value of the deviation over the full scale in the number of LSB units [Johns97][Sansen06].

Settling time is the time needed for the output to settle to a value within its specified error limits in response to a step function at the input. It is normally given in μs for the output gain of 1 of the amplifier. **Glitch** represents the area of the unwanted signal generated at the output when the input changes by

one bit. Normally the change is measured when the largest number of bits changed, for example, from 0x7FF to 0x800 for a 12-bit D/A converter. It is given in $nV \times s$.

The same frequency domain characteristics are used here as those described in Section 4.5.2 for A/D converters.

4.6.1.3 Integrated special-purpose D/A converters

Special purpose integrated circuits based on D/A converters include:

- Waveform generators
- Bioimpedance measurement chips
- D/A converters specialized in audio or video signals

Waveform generators are used in many applications, including frequency stimulus, bioimpedance measurements, sensor applications for proximity and motion, clock generators, and so on. These waveform generators can produce sine, triangular, and square wave outputs. The output frequency and phase are commonly software programmable. An example of a circuit is AD9837 by Analog Devices, which can be tuned to 0.02 Hz resolution with up to 5 MHz frequency. Basic waveform generators are based on the sequential reading of waveform amplitudes from an internal lookup table and converting them into an analog signal using a D/A converter. For example, the AD9837 has a 10-bit D/A converter.

Waveform generation based on direct digital synthesis (DDS) allows for generating sine waves with precise phase and frequency control, including single-frequency sinewave and sweeping sine wave signals. Frequency resolution and maximum frequency are normally much better than the resolution and frequency achieved using other types of waveform generators.

Bioimpedance measurement chips are based on DDS techniques that allow for generating sinewave signals. They are used for electrochemical analysis, bioelectrical impedance analysis and impedance spectroscopy. The waveform generator provides a signal of known frequency at the output of the chip that is used to excite an external complex impedance. The response signal from the impedance is sampled by an A/D converter. An example of that is the AD5933 integrated circuit by Analog Devices.

4.6.2 Pulse width modulation

Pulse width modulation (PWM) generates square-wave pulses of different widths. The width of the pulse, sometimes called pulse width offset, is commonly proportional to the amplitude of the input signal. PWM is used to control motors or to power LEDs. The main reason for using PWM is that it allows for controlling the average amount of power delivered to a load or the output. They are also used for voltage regulation and modulation in communications.

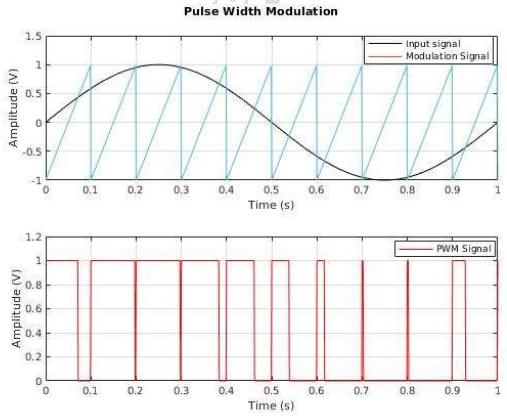


Fig. 4.29 PWM signal generation. The upper figure shows the input signal and the triangular modulation waveform, while the lower figure shows the PWM signal output.

A PWM system normally has several parameters for tuning, including the PWM period (reciprocal of the pulse frequency), the pulse width offset and pulse delay time. Pulse delay time represents the shift in time compared to the pulse starting at 0 s. The values can be given in percentages of PWM period or seconds. Pulse width offset D is given in percentage of the PWM period T. Sometimes, offset is also given in seconds. PWM output signal $y(t)$ is logic one (y_{max}) during the time DT and logic zero (y_{min}) during the period $(1-D)T$. The average amplitude of the signal $\bar{y}$ at the output of PWM is:

$$\bar{y} = \frac{1}{T}\int_0^T y(t)dt = \frac{1}{T}\int_0^{DT} y_{max}dt + \frac{1}{T}\int_{DT}^T y_{min}dt = D\,y_{max} + (1-D)y_{min}$$

When $y_{min} = 0\ V$ then $\bar{y} = Dy_{max}$. The simplest way to generate a PWM signal $y(t)$ is to use a triangular wave generator as a modulation waveform and a comparator. When the amplitude of the input signal is larger than the amplitude of the modulation waveform, the output is logic one – otherwise, the output is a logic zero. Fig. 4.29 shows a 10 Hz modulation waveform in blue. The input signal is the sine wave with a frequency of 1 Hz, shown as a black line in the upper figure. The lower figure shows the output PWM signal.

PWM to voltage conversion can be done by integrating the PWM signal by connecting the PWM signal to a lowpass filter. This emulation of D/A converter has traditionally been done for low-speed, low-resolution applications. The accuracy of this circuit depends on the properties of the lowpass filter. If the lowpass filter has a bandwidth that is too small, then it will take much time for the signal to change from one state to the next. On the other hand, if the bandwidth of the filter is high, then the signal at the output of the filter will oscillate around the mean value of the PWM signal, which means that the resolution of the emulated D/A converter will be low. Therefore, this solution is used in low-cost microcontroller-based applications where the PWM signal is generated at the output of the microcontroller [Alter08] – please see Problem 4.23. There are also PWM to voltage integrated solutions mainly based on converting PWM signal into a binary signal and then doing D/A conversion. In that case, good signal resolution at the output can be achieved.

4.7. Other components of the system

Until now, we introduced transducers, amplifiers, analog filters, A/D and D/A converters. Very often, these components are combined to form **sensors**. We define a sensor as a device that converts the physical measurand into voltage or current output. Sensors will be introduced in Chapters 6-10 when we discuss different devices. The sensor's output can be analog; in this case, the sensor is connected to a processing unit through an A/D converter. The sensor integrated circuit can also contain an A/D converter producing a digital signal at the output. The digital-output sensor is connected with a processing unit through a digital communication interface. Common interfaces that are used nowadays in wearable devices include SPI and I^2C. I^2C, or Inter-Integrated Circuit, is a chip-to-chip interface supporting two-wire communication. SPI, or Serial Peripheral Interface, is a synchronous serial data link standard that operates in a full-duplex mode. Both interfaces connect the microcontroller with relatively slow peripherals, A/D and D/A converters and digital sensors.

Other system components include a processing unit, power management unit, battery and battery charger, and digital electronic components. Some of these components will be introduced in Chapter 11.

Wearable devices are designed as embedded systems. **Embedded system** is a special-purpose computer system optimized to execute several specialized functions while the optimizations normally include [Valvano22]:

- software designed for the particular hardware, including available sensors and other components
- real-time constraints meaning that certain processing tasks need to be completed before the deadline
- need to minimize memory requirements since the amount of memory in the embedded system is normally small in comparison with memory available on personal computers
- need to minimize power consumption.

Microcontrollers (MCU) are used in embedded systems to perform a certain task, handle communication and control other hardware components. A microcontroller normally contains a relatively simple central processing unit (CPU) combined with peripheral components such as memories, I/O devices, and timers [Valvano22]. Some of the components commonly integrated on a chip are:

- Interrupt Controller
- On-Chip Memory
- Power management control unit that is used for entering/leaving power-down modes, and enabling or disabling the peripherals
- Direct Memory Access (DMA) Controller that allows for data transfer between the memory and peripherals without using the CPU
- One or more A/D converters
- One or more D/A converters
- Comparators that compare the analog input with a preset threshold and provide a binary output that is logic one if the input signal is greater (or smaller depending on the implementation) than the threshold
- Multiple timers/counters that can generate interrupts after some programmed time intervals
- Real-Time Clock (RTC) that is used to track clock time and calendar date, and it is normally turned on all the time
- I^2C and SPI buses for connecting MCU to other peripherals

Some MCUs also have integrated Bluetooth or other communication modules. As an example, ARM® Cortex-M0+ core can run up to 48 MHz, has on-chip 512 KB flash memory and on-chip 128 KB of random access memory (RAM).

Digital signal processors are processors designed for completing signal processing tasks such as filtering or computing Fast Fourier Transform (FFT). These tasks involve repetitive numeric calculations, such as multiple and add/accumulate (MAC) operations. Digital signal processors implement fixed-point or floating-point algorithms requiring high memory bandwidth for the streaming sensor data. Modern digital signal processors include special hardware for performing MAC operations, can execute multiple operations and memory accesses per clock cycle, and have multiple addressing modes to support the implementation of algorithms such as FFT.

4.8. Summary

This chapter focuses on the electronics required to interface the sensors with processors. We covered bridge circuits, operational amplifiers, analog filters, and A/D converters. In addition to the data acquisition path, we briefly analyzed circuits required to generate signals and drive the loads. These circuits include D/A converters and PWM circuits.

In this chapter, we introduced a number of newer solutions that are commonly used in design nowadays. These integrated single-chip solutions include multiple components we studied in this chapter placed in one chip. Examples include transimpedance amplifiers, different types of bridges, waveform generators in D/A converter section, capacitance to digital and time to digital converters in the A/D converter section, and so on. These should give the readers ideas about current trends in the industry.

There are several limitations in this chapter. Sometimes, examples of integrated solutions from industry are chosen. These examples are chosen randomly without the intention to favor any particular company – nevertheless, it turned out most examples are from Analog Devices. Power consumption is not analyzed, which should have been done if these components are used in wearable biomedical devices. Digital electronics is not introduced here, and we assume that the majority of digital processing will be performed in software on a computer, processor, or microcontroller. Processor and microcontroller architectures are not discussed.

4.9. Problems

Please note that questions that start with * are not covered in the book. They are added for the readers interested in exploring different topics further.

4.9.1 Simple questions

Questions: Wheatstone bridge

4.1. Describe the Wheatstone bridge and describe how it is used to connect different transducers.
4.2. Describe configurations and derive an input-output relationship for bridges with 1, 2 and 4 transducers in the bridge. Compare results.
4.3. What can be done when it is not possible to place transducers so that two of them increase resistances and two decrease resistances?
4.4. How are capacitive transducers connected to the amplifier?
4.5. *Describe temperature effects on the bridge. How is temperature compensation done?

Questions: Instrumentation and differential amplifiers

4.6. What are differential gain, common mode gain and common mode rejection ratio of amplifiers? What are their typical values for amplifiers used in ECG and EEG?
4.7. Derive the differential gain and the common mode gain of an instrumentation amplifier.
4.8. Why is it better to use an integrated instrumentation amplifier in a chip and not build your own using operational amplifiers and resistors? Discuss the need to match resistors up to 0.02% accuracy.
4.9. Describe programmable gain instrumentation amplifiers.
4.10. Is there a relationship between the gain and the bandwidth of the instrumentation amplifier?

4.9.2 Problems

4.11. Derive the output voltage and the output current of a circuit model presented in Fig. 4.2a).
4.12. Derive the formulas (4.5) and (4.6) for the output voltage of the charge amplifier.
4.13. In Example 4.3, the interpolated signal has a fundamental frequency of 2 Hz. Why is then interpolated sine wave at 2 Hz shifted by 180°?
4.14. Compute linearity error $\%e_{L_{max}}$ for the quarter bridge using both the terminal and the best-fit straight-line methods described in Chapter 3. Please note that the nonlinearity error computed here is for the bridge itself without including the transducer.
4.15. Consider a system for monitoring breathing using an accelerometer shown in Example 4.2. The accelerometer is placed on the subject's chest. Please assume that the breathing signal is periodic and that it is causing changes of 10 mg in one of the axes of the accelerometer (see, for example, [Schipper21]). What would be the amplitude of the voltage V_{o1} and V_o in Fig. 4.12.
4.16. Show expressions for the gain of the PGA shown in Fig. 4.15. Modify the PGA to support the gain of 4 as well.

4.9.3 Simulations

4.17. Modify the equivalent circuit model shown in Fig. 4.2a) to include the offset voltage, input bias current noise of the amplifier. Find a data sheet of a precision amplifier of your choice to obtain realistic values of these parameters.
4.18. Draw V_0 versus v_{in} when $\Delta R/R$ changes from -10% to 10% in the steps of 1% for the resistive bridge with:

a) One sensor
b) Four sensors

4.19. The ramp generator is shown in Fig. 4.30. The input signal is a pulse with a frequency is 1 kHz, 50 % duty cycle, a minimum amplitude of -1 V and a maximum amplitude of 0 V. The output is a triangular shape pulse with a minimum amplitude of 0 V and maximum amplitude V_{max}. Implement this ramp generator in Simscape and show how you selected components to get the desired output.

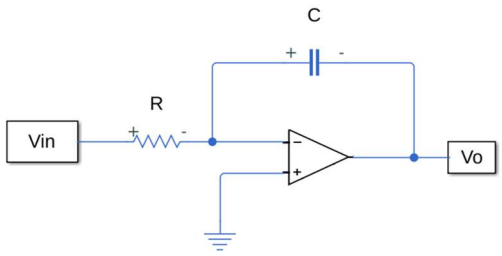


Fig. 4.30 Integrator (ramp amplifier)

4.20. Consider formula (4.4) for interfacing a capacitive sensor that changes its capacitance with the distance between the electrodes. Then, compute the formula for the output voltage vs. distance change between the electrodes.
4.21. Show the Bode plot for the charge amplifier in Fig. 4.12. Compare lower and upper cut-off frequencies with the ones computed in Example 4.2. In order to do this, make sure that you label input and output signals in the circuits by clicking on the line of interest and then selecting Linear Analysis Points. After selecting the input and output signal, go into the Frequency Response app in Simulink and select Bode plot.
4.22. Modify the code for **Example 4.3** for the following sampling rates 10 Hz, 20 Hz, 27 Hz, 30 Hz.
4.23. This question is related to PWM signal generation.
a) Implement PWM signal in Simscape with the pulse with offset D=50%, $T = 10\mu s$ and $y_{max} = 3.3\ V$ and $y_{min} = 0V$ followed by a first-order passive lowpass filter. Analyze the output of the filter when the cutoff frequency is i) 50 kHz, ii) 1 kHz, iii) 10 MHz.
b) Assume that this circuit is used as a D/A converter. Analyze the performance of this converter for cases i), ii), and iii) above.

4.10. Additional resources

In this section, we refer to several relevant resources for further reading. However, please note that this list is not comprehensive and that many excellent and relevant resources might have been omitted unintentionally.

A comprehensive overview of instrumentation amplifiers is given in [Kitchin06]. Active filters are detailed in the book [Wanhammar09]. A very comprehensive resource for A/D and D/A converters is [Kester05a]. An excellent book that focuses only on A/D converters is [Pelgrom17].

Many excellent books are available for an introduction to the sampling theorem, antialiasing, and other topics related to signal processing, including [Oppenheim98].

A good practical resource for learning about embedded systems is [Valvano22].

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