BT University

DIGITAL LOGIC CIRCUIT

B TECH ELECTRICAL & ELECTRONICS ENGINEERING

PROFESSIONAL ENGINEERING CREDITS ASSESSMENT & CONTINUIOUS INTERNAL EVALUATION

PART I

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 2 MARKS)

ANSWER ANY 10 QUESTION

1. Define binary logic?
2. What are the basic digital logic gates?
3. What is a Logic gate?
4. Give the classification of logic families.
5. Which gates are called as the universal gates? What are its advantages?
6. Classify the logic family by operation?
7. Mention the important characteristics of digital IC's?
8. Define Fan-out?
9. Define power dissipation?
10. What is propagation delay?
11. Define noise margin?
12. Define fan in?
13. What is Operating temperature?
14. What is High Threshold Logic?
15. Define combinational logic
16. Explain the design procedure for combinational circuits

17. Define Half adder and full adder

18. Define Decoder?

19. What is binary decoder?

20. Define Encoder?

21. What is priority Encoder?

22. Define multiplexer?

23. What do you mean by comparator

PART IA

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 6 MARKS)

ANSWER ALL QUESTION

1. Obtain the minimum sop using QUINE- McCLUSKY method and verify using K-map
F=m0+m2+m4+m8+m9+m10+m11+m12+m13

2. Reduce the following using tabulation method.

F=m2+m3+m4+m6+m7+m9+m11+m13

3. Design A Full Adder And A Full Subtractor

4. a) Design a 2 bit magnitude comparator.

b) Explain the operation of 4 to 10 decoder

5. Design a 4-bit binary to excess-3 converter using the unused combinations of the code as don't care conditions. Represent the converter using logic diagram

PART II

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 2 MARKS)

ANSWER ANY 10 QUESTION

1. What are the classification of sequential circuits?

2. Define Flip flop.

3. What are the different types of flip-flop?

4. What is the operation of D flip-flop?

5. What is the operation of JK flip-flop?

6. What is the operation of T flip-flop?

7. Define race around condition.

8. What is edge-triggered flip-flop?

9. What is a master-slave flip-flop?

10. Define rise time.

11. Define fall time.

12. Define skew and clock skew.

13. Define setup time.

14. Define hold time.

15. Define propagation delay.

16. Define registers.

17. Define sequential circuit?

18. Give the comparison between combinational circuits and sequential circuits.

19. What do you mean by present state?

20. What do you mean by next state?

21. State the types of sequential circuits?

22. Define synchronous sequential circuit

PART IIA

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 6 MARKS)

ANSWER ALL QUESTION

1. Design a mod-10 synchronous counter using Jk ff. write excitation table and state table.

2. a) Write the excitation tables of SR, JK, D, and T Flip flops

   b) Realize D and T flip flops using Jk flip flops

3. Design a counter with the following repeated binary sequence:0, 1, 2, 3, 4, 5, 6.use JK Flip-flop.

PART III

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 2 MARKS)

ANSWER ANY 10 QUESTION

1. Define Asynchronous sequential circuit?

2. Give the comparison between synchronous & Asynchronous sequential circuits?

3. The following wave forms are applied to the inputs of SR latch. Determine the Q waveform Assume initially Q = 1

4. What is race around condition?

5. Give the comparison between synchronous & Asynchronous counters.

6. The t pd for each flip-flop is 50 ns. Determine the maximum operating frequency for MOD - 32 ripple counter

7. What are secondary variables?

8. What are excitation variables?

9. What is fundamental mode sequential circuit?

10. What are pulse mode circuit?

11. What are the significance of state assignment?

12. When do race condition occur?

13. What is non critical race?

14. What is critical race?

15. When does a cycle occur?

PART IIIA

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 6 MARKS)

ANSWER ALL QUESTION

1. Explain the difference between synchronous and asynchronous sequential circuits

2. Derive the transition table for the asynchronous sequential circuit shown below. Determine the sequence of internal states Y1Y2 for the following sequence of inputs x1x2: 00,10,11,01,11,10,00.

3. Design a circuit with input a and b to give an output z=1 when AB =11 but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and output map in which transient state is included

4. Design an Asynchronous sequential circuit using SR latch with two inputs A and B and one output y. B is the control input which, when equal to 1, transfers the input A to output y. when B is 0, the output does not change, for any change in input

PART IV

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 2 MARKS)

ANSWER ANY 10 QUESTION

1. Mention the classification of saturated bipolar logic families.

2. Explain ROM

3. What are the types of TTL logic?

4. Define address and word.

5. What is programmable logic array? How it differs from ROM?

6. Explain EPROM.

7. Give the classification of PLD's.

8. Define PROM.

9. Define PLA

10. Define PAL

11. Why was PAL developed ?

12. Why the input variables to a PAL are buffered

13. What does PAL 10L8 specify ?

14. Give the comparison between PROM and PLA.

PART IVA

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 6 MARKS)

ANSWER ALL QUESTION

1. a) compare the various digital logic families.

   b) Write notes on FPGA.

2. Write notes on the characteristics and implementation of the following digital logic families.

   i) ECL ii) TTL

3. Write short notes on semiconductor memories

4. Discuss on the concept of working and applications of following memories

   i) ROM ii) EPROM iii) PLA

5. a) Explain in detail about PLA with a specific example.

   b) Explain with neat diagrams RAM architecture

PART V

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 2 MARKS)

ANSWER ALL QUESTION

1. What do the acronyms VHDL and VHLSI stand for?

2. What are the different types of modeling VHDL?

3. What is packages and what is the use of these packages

4. What is variable class ,give example for variable

5. Name two subprograms and give the difference between these two.

6. What is subprogram Overloading

7. write the VHDL coding for a sequential statement (d-flipflop)

8. What are the different kinds of the test bench?

9. What is Moore FSM

10. Write the testbench for and gate

PART VA

UNIVERSITY EXAM QUESTION PATTERN – 6 MARK (EACH QUESTION CARRIES 6 MARKS)

ANSWER ALL QUESTION

1) Write a HDL code for state machine to BCD to ex–3 codes Converter.

2) Write a behavioral VHDL description of the 4 bit counter.

3) (I) Write VHDL code for a full sub tractor using logic Equation

(II) Write a VHDL description of an S-R latch using a process

4) Write a HDL code for 8:1 MUX using behavioral model

5) (I) Write an HDL data flow description of a 4 bit adder subtractor of Unsigned numbers use the conditional operator

(II) Write the HDL gate level description of the priority encoder

END