# Task II

## Design and Implementation of Combinational Logic Circuit

a. **Write a truth table and logical expression for Full adder and Full subtractor**

b. **Simplify the expression using K-Map,**

c. **Draw the logic diagram of Full adder and full subtractor**

*d.* **Write a Verilog code for Full adder and Full Subtractor in Behavior level, Structural level, Data flow level and Conditional operator with test bench and verify its output. (Verilog code must have line by line comments)**