Design of CMOS Instrumentation Amplifier with Improved Gain & CMRR for Low Power Sensor Applications

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Abstract. This proposed work reveals a high performance instrumentation amplifier based on operational amplifier (op-amp) for low power applications. This instrumentation amplifier (IA) is designed for low power while maintaining the high gain, high CMRR, low noise as well as other design constraints. The Instrumentation amplifier contains two identical two stage op-amps at the input (gain) stage and one difference amplifier at output stage. By using operational amplifier at the gain stage in saturation region and difference amplifier at the output stage in subthreshold region to achieve high gain and CMMRR. Aspect ratio (W/L) plays very important role in achieving these designing constraints. In this paper our main focus is to achieve high gain and high CMRR with moderate noise and less power performance for modern circuit's applications. The whole instrumentation amplifier schematic is designed and simulated at 180nm CMOS technology using Cadence Spectre tool. The IA achieve an overall gain and CMRR of 79.16 dB and 98 dB respectively. The comprehensive (overall) power consumed by this instrumentation amplifier design is 409µW and input referred voltage noise is 9.65µV/√Hz which is advisable for biomedical signal processing as well as low power sensor applications.

***Index Terms*--- Instrumentation amplifier, Op-Amp, Gain, CMRR, Input & Output Referred Noise.**

I. INTRODUCTION

The trends of technological development are heavily focused on improving and expanding the integration of digital processing in everyday life. This development demands that analog circuitry keep up with the phase. CMOS instrumentation amplifiers (IAs) have pumped up surprisingly for looming sensor circuit applications such as integrated strain sensors, hall sensors, thermocouples, micro-electromechanical system, multichannel sensing systems and integrated biosensors [1]. Sensors are used to translate information from various physical domains like thermal, mechanical, and magnetic to information measurable in electrical domain. This electrical signal is generally an analog signal and needs to be translated to digital signal for further signal processing. The system involved in the chain of converting the analog signal from sensors, to digital signal is called sensor readout system. In all these applications, low power consumption is aimed to reduce its cost and as battery point of view, longer operating lifetime [2].

Instrumentation amplifier models a crucial part of the low power applications since it demands to individuate noise and small amplitude signal which is desired [3]. The Transforming circuitry resides of an instrumentation amplifier which is applicable for precision amplification of DC/AC signals in differential mode while eliminating common mode signal values. Over large voltage range, instrumentation amplifiers that perform on 5V are advantageous [4]. The Well-known design used in a low power sensor system, is an operational amplifier (Op-Amp), must manifest low power consumption and small input voltage referred noise, high Common Mode Rejection Ratio (CMRR). In this proposed work, a low voltage, low noise and high CMRR operational amplifier for portable monitoring system is described. The proposed op-amp is having an innate capacity to work under 1.8-V supply, has required design constraints like high gain & CMRR and low voltage noise. Devices may pertain to different inversion region like weak, moderate and strong. Out of these three regions, transistor (MOSFET) functioning in saturation region is most convenient for low power applications where devices are regulated either at low voltage, current or both [5].

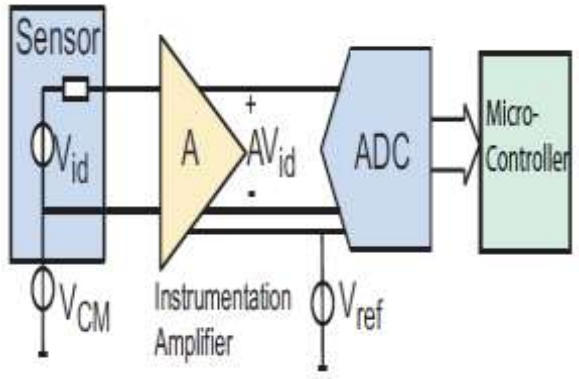

Fig.1. Block diagram of typical sensor readout system

Fig. 1 shows a typical sensor readout system whose output assumed to be in voltage. The differential voltage (Vid) from the readout system is amplified by the amplifier (A) and given to an Analog to Digital Converter (ADC). ADC converts the information to digital domain. This digital data can be processed by a micro-controller. As typical sensor signals are very small (in μV), an amplifier A is used to increase the signal before passing it to ADC. The main functions of Instrumentation Amplifier in this system are to

- Amplify the differential voltage (Vid).
- Reject the sensor common mode voltage (VCM).
- Level shift to ADC reference voltage (Vref).

As these amplifiers are used to detect very small input differential signals, the input referred errors (due to offset & noise) of such amplifiers should be well below the minimum input signal.

Section II and Section III deals with ideal three op-amp structure and proposed instrumentation amplifier (two op-amp and one differential amplifier). Section IV explains the simulation results implemented in cadence spectre tool with 180nm CMOS technology. Section V, gives the conclusion.

II. INSTUMENTATION AMPLIFIER DESIGN TOPOLOGY

Instrumentation amplifier can be designed from an op-amp circuit but the behavior of instrumentation amplifier is intensely different than an op-amp and difficult to design precisely from single op-amp circuit. Instrumentation amplifier can be designed by several different ways. The commonly used techniques are difference amplifier, two op-amps, three op-amps, switched capacitor, capacitively coupled, current mode, resistive feedback and current feedback instrumentation amplifier.

The classical three op-amp instrumentation amplifier shown in [6] having inputs V_{IN-} & V_{IN+} defined by the input polarity of difference amplifier A_3. These inputs can be categories as common mode voltage and difference voltage. These voltages cab be expressed as:

$V_{CM} = (V_{IN-} + V_{IN+})/2$ and $V_D = V_{IN+} - V_{IN-}$ (1)

Now input voltages can be calculated in terms of common mode and difference voltage as:

$V_{IN+} = V_{CM} + V_D/2$ and $V_{IN-} = V_{CM} - V_D/2$ (2)

Difference voltage V_D is applied across gain resistor as shown in figure 4 to calculate current, I_D

$I_D = (V_{IN-} + V_{IN+})/R_G = V_D/R_G$ (3)

The output voltage of first stage op-amps are

$$V_1 = V_{CM} - \frac{V_D}{2} - I_D.R_F \quad \text{and}$$

$$V_2 = V_{CM} + \frac{V_D}{2} + I_D.R_F \quad (4)$$

Replacing the current value from equation 3 into equation 4

$$V_1 = V_{CM} - \frac{V_D}{2} * G_1 \quad \text{and}$$

$$V_2 = V_{CM} + \frac{V_D}{2} * G_1 \quad (5)$$

Where Gain, $G_1 = 1 + (2*R_F/R_G)$

Equation 5 represent that only difference voltage term is amplified by gain and common mode voltage is passes input stage with unity gain. The output of difference amplifier after the second stage can be describe by

$V_0 = (V_2 - V_1)*G_2$ where $G_2 = R_2/R_1$ (6)

by using equation 5&6 the transfer function of instrumentation amplifier can be expressed as:

$$\frac{V_0}{V_D} = G_1 * G_2 = G_{total} \quad (7)$$

Standard instrumentation amplifier using a unity gain difference amplifier in the output stage, however, can limit the input common mode range significantly [6]. The three op-amp IA suffers from a limited Common Mode Rejection ratio(CMRR) due to resistor mismatch [7].It does not provide a good power noise tradeoff A switched-capacitor IA can be used to improve the CMRR, but it suffers from low input impedance. A CFIA can achieve better CMRR and input impedance as compared to three op-amp and Switched Capacitor IA.

III. PROPOSED INSTRUMENTATION AMPLIFIER

Instrumentation Amplifier (IA) can be implemented in different ways. In the previous section we have discussed some of the commonly used topologies. Fig. 2 shows block diagram of 3 op-amp IA. Our main concern while designing an IA is to reduce the interferences in the form of common mode voltage. The block diagram of proposed complete IA shown in fig. 2. The first 2 op-amp at the gain stage are identical and their transistor level diagram shown in fig. 3. The two stage op-amp includes a bias circuit, a differential amplifier, a second gain stage and a compensation circuit [7].

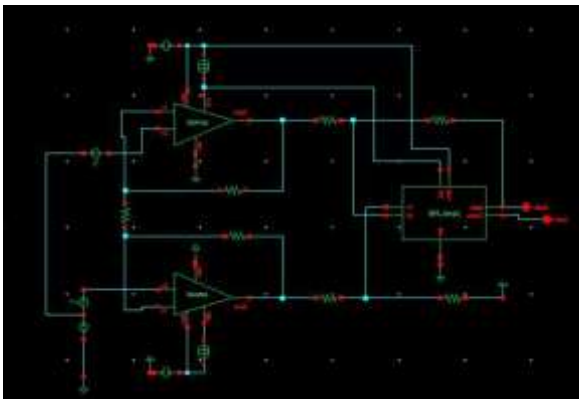

Fig. 2. Proposed Instrumentation amplifier block diagram

The differential amplifier stage provides gain to improve the performance in terms of noise and offset. The bias circuit is used to establish the operating point for all transistors in saturation as well as subthreshold region. The main motto of compensation circuit is to maintain the stability when negative feedback is applied to the op-amp. The second stage of IA is differential stage whose transistor level diagram shown in fig. 4.

In operational amplifier load capacitor C_L=10pF and miller capacitance (compensation capacitor) C_C=550fF.

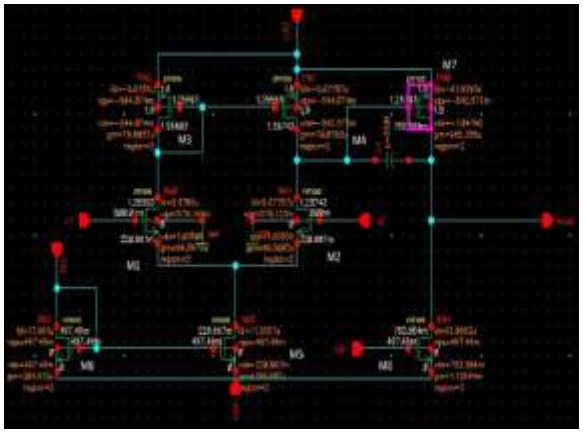

Fig. 3. CMOS implementation of two stage Op-Amp

In the analysis of instrumentation amplifier 1.8volt power supply with bias current Ibias=20µA is used.

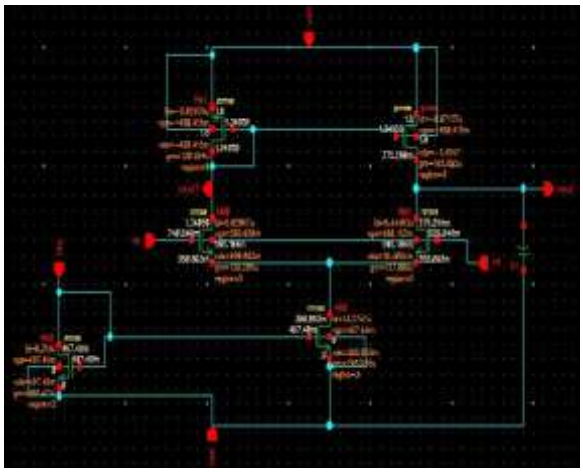

Fig. 4. CMOS implementation of differential amplifier

The first two op-amps are used in buffer mode to provide high input impedance followed by difference amplifier. All the transistors at stage one in saturation region and stage two transistors are in subthreshold region. Aspect ratio of all the transistors are shown in table 1. This aspect ratio plays very important role in making transistors in saturation and subthreshold region. The value of resistive network of IA shown in fig. 2 R_G, R_F, R_1 and R_2 are 100ohm, 100Mohm, 10Kohm and 1Mohm respectively.

Table 1: Aspect ratio for CMOS IA

Transistors	Block	Aspect Ratio
M1, M2	Op-amp	6µ/1µ
M3,M4	Op-amp	14µ/1µ
M5,M6	Op-amp	12µ/1µ
M7	Op-amp	32µ/200n
M8	Op-amp	37.5µ/500n
M1,M2	Diff. amp	8µ/200n
M3,M4	Diff. amp	20µ/200n
M5	Diff. amp	10µ/200n
M6	Diff. amp	5µ/200n

IV. SIMULATION RESULTS

A. AC ANALYSIS OF PROPOSED INSTRUMENTATION AMPLIFIER

AC analysis has been done for proposed IA circuit using cadence spectre tool at 180nm gpdk CMOS

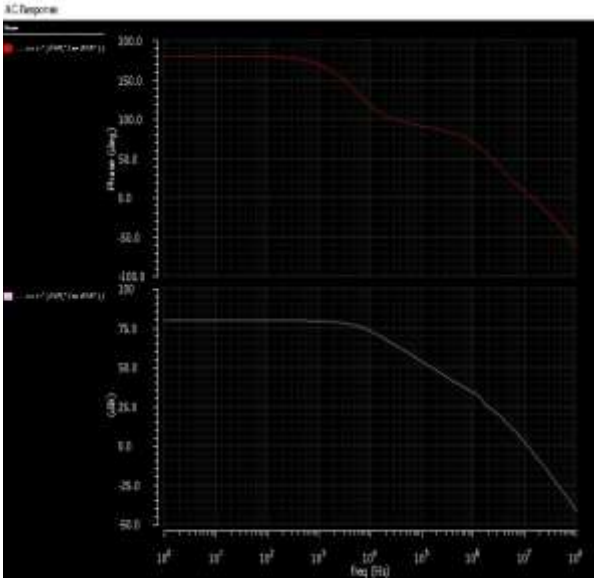

Fig. 5. Gain and phase response of IA

technology.

In this procedure supply voltage and biasing parameters (biasing voltage and current) are same as discussed above. By using this analysis gain, phase response as well as the CMRR are measured. Fig. 5 shows the phase and gain response of proposed instrumentation amplifier. CMRR of the proposed IA is the ratio of A_d (differential gain) and A_c (common mode gain). So the value of gain and CMRR achieved by this IA are 79.16dB and 98dB respectively. The I/O voltage referred noise data has been plotted in cadence spectre simulator tool. Noise analysis has been performed with a 1mV sinusoidal signal with common mode voltage of 0.8V at the input terminal. The input referred noise plot is shown in fig. 6 gives a peak value of 9.65µV/√Hz and output noise is 5.46mV/√Hz.

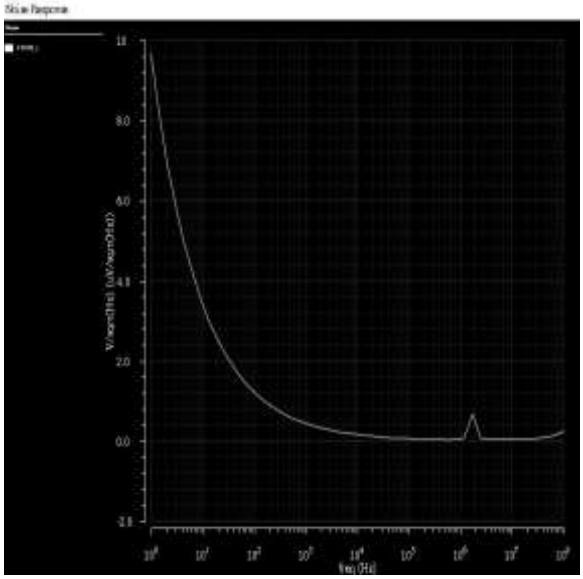

Fig. 6. Input referred voltage noise of IA

Table 2 represents a comparison state of art of the proposed instrumentation amplifier (IA) design with some existing literature designs. The demanding design constraints taken into discussion for comparison the gain, CMRR, gain bandwidth, power dissipation, input referred voltage noise, output referred voltage noise for proposed design of IA and other literature. The comparison shows that effective increment in gain, CMRR and gain bandwidth product with moderate noise and power performance.

Table 2: Comparison of present state-of-the-art

Parameter	This Work	[8]	[12]	[9]	[10]	[11]
Technology (μm)	0.18	0.18	0.5	0.5	0.18	0.8
Gain (dB)	79.16	67.7	45	19.9	19.6	40
CMRR (dB)	98	92	75	>110	92	NA
Gain (MHz) Bandwidth	9	1.75	1.1	20khz	100	NA
Power (μW) Dissipation	409.14	263	283	NA	NA	122
Input referred voltage noise(V/√Hz)	9.65μ	89n	22n	175n	22.8M	NA
output referred voltage noise(V/√Hz)	5.46m	1.75μ	5.63p	NA	NA	NA

V. CONCLUSION

In this paper, the designing concept for instrumental amplifier (IA) using modified 3 op-amp architecture with different transistor sizing for low voltage and low power sensor applications is unveiled. The design triumph comparatively improved gain & CMRR as compared to the state of art .The design also ensures moderate noise and power one of the main circuit application. The main focus of the future work is to reduce the offset and noise while maintaining the required design constraints.

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